Design methodologies for high-speed CMOS photoreceiver front-ends

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Abstract—A hierarchical design methodology for wide bandwidth photoreceiver front-ends is presented in this paper. We propose a unified approach for both optoelectronic and electronic components in the front-end. This approach enables us to improve system performance by considering design constraints in both domains, which is impossible with traditional segregated design flows. Based on a hierarchical synthesis platform aimed at fast multi-domain system design automation, we optimize the photodiode structure and CMOS transimpedance amplifiers for different technology nodes with accurate performance prediction.

Index Terms— photodiode, transimpedance amplifier, design methodology, optical link

I. Introduction

The increasing demand for high speed data communication in the telecommunications, networks and computing sectors has engendered needs for low cost solutions with channel bandwidths in the Giga-Hertz range. Optical communication systems provide these services for long-haul communication, local networks, board-to-board, chip-to-chip and in the future even on-chip communication. Thanks to the monolithic integration of optical and electronic components in OEICs (**O**pto**E**lectronic **I**ntegrated **C**ircuit), superior performance can be achieved with significant cost reduction.

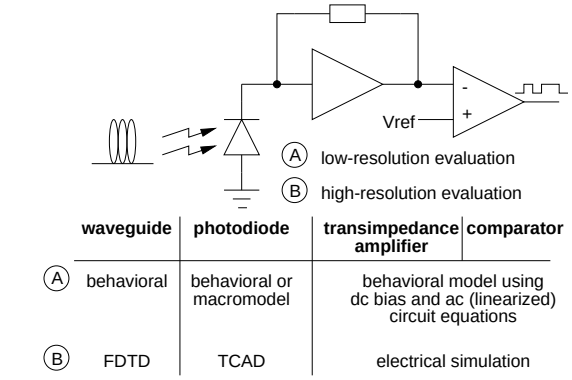
A typical optical link transmits digital signals but is composed of three components of essentially analog nature [1]:

(i) the transmitter, which converts the digital electrical input to an optical signal;

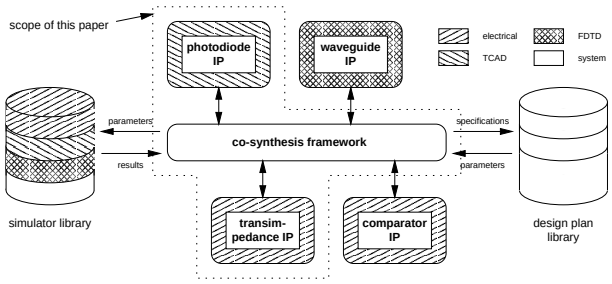
(ii) the transmission medium, representing waveguide, fiber or free space between optoelectronic components;

(iii) the receiver, which converts the optical signal to a digital electrical output.

Of these, the receiver is the part that presents the greatest limit to high-speed performance, because in general the photodiode capacitance at its input is large and directly influences the bandwidth of the system. The receiver is composed of several functional blocks; in this work, we focus on the photoreceiver front-end. Sizing of such blocks is a problem representative of many for which existing design technology is inadequate due to their *complexity* and *heterogeneity*. Concerning the complexity, a simple photoreceiver can be implemented with a minimum of two blocks. At high frequencies we need to take all parameters into account, and consequently the set of design parameters increases. Efficient evaluation of these circuits is increasingly difficult and requires long CPU times.



(a) System schematic



(b) Cosynthesis backplane showing multiple simulators and design plans

Fig. 1. Multi-domain system example: integrated optical receiver

Generally, sizing at transistor level becomes prohibitive above a certain number of transistors since the number of design parameters, N, is of the same order of magnitude as the number of transistors in the block. If the number of solutions visited for each individual design parameter is represented by s, the time necessary for each evaluation carried out during the design process by T_e, and the parameter generation time by t_g, then the total design time t_d is:

$$t_d = (T_e + t_g) \prod_{i=1}^{N} s_i \qquad (1)$$

which is clearly impractical for large blocks. For this reason, we must use techniques to simplify the design problem and reduce its complexity; design tools capable of handling design problems through several hierarchical loops are there-

fore necessary. As concerns heterogeneity, the photoreceiver contain two components of different physical type, a photodiode (optical type) and a transimpedance amplifier (electrical type).

For synthesis, this is the greatest problem, since no existing tool is capable of taking heterogeneity into consideration, meaning in our case that the OEIC system is not optimized and the design process inefficient. To illustrate these last points, fig. 1(a) shows the receiving end of an integrated optical link. The performance of this link can be simulated (A) with parameterized behavioral component models to verify the functionality at the system level, but this gives no clue as to the physical consequences (area, power, parasitics) of the choice of parameters. Such information can only be obtained by designing the various components and evaluating with methods appropriate to the domain (B).

Our solution addresses both problems and consists of (i) carrying out a top-down design space exploration using behavioral models to the physical level, (ii) physical sizing linking directly from a co-synthesis backplane to the various evaluation tools, as shown in fig. 1(b), and (iii) subsequent bottom-up design verification using model parameter extraction. Our methodology has been completely integrated in an in-house synthesis platform. Key to this approach is the concept of analog intellectual property (IP) blocks. This is an asset characterized i) economically, by the notion of ownership (commercial value, security and protection) and ii) scientifically, by the notion of re-use in several forms [2].

In this paper we present in detail the various stages that we have used to implement a complete design methodology for the photoreceiver. Section II describes the structure of the IP "blocks" and their use in the design process. In section III, we present the sizing procedure for each individual block including a global automated verification stage in section IV. We present the results of our work in section V.

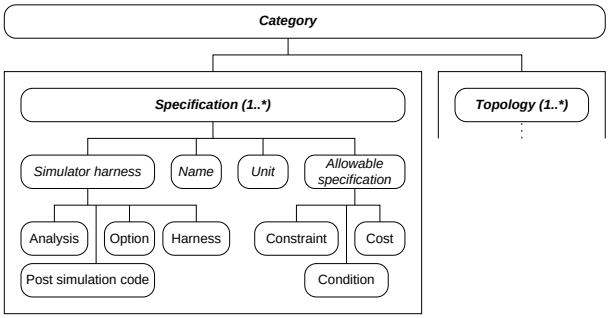
II. Design process

In the introduction we have explained the need for a hierarchical design flow to solve problems related to the complexity and heterogeneity of high-performance systems. To this end we require an automated design flow enabling hierarchical specification propagation. In this section we introduce the basic building block, which must be able to capture information relating to the design of a particular structure, i.e:

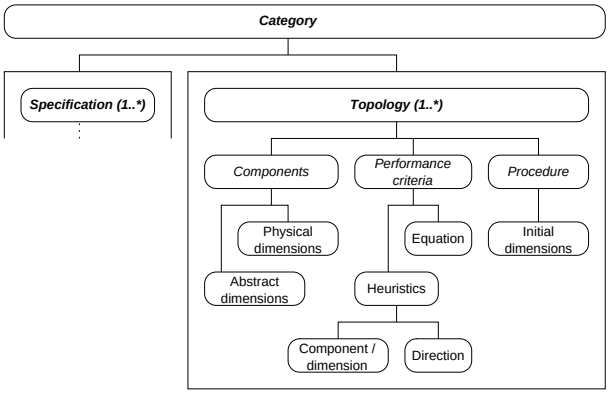
- how it will be specified and what are its performance criteria
- how it will be designed and what are its parameters
- how it will be evaluated

A. IP structure

For our design methodology, we will be using optimization algorithms within design plans (described in section B), which require the formulation of an error function to be minimized. The way in which we translate user specifications into an exploitable error function is critical to the success



(a) Specification structure



(b) Topology structure

Fig. 2. Domain-independent IP structure

of the design phase. Since specifications actually belong to a *class* of topologies rather than to one single topology, we have developed a specification structure depending on a category. Topologies belonging to a given category inherit this common set of specifications, which will be quantified by the user during synthesis runs (fig. 2(a)).

We classify specifications into three types, each of which contributes to the global error function to be minimized in different ways. In the following definitions, ε represents the individual error function contribution of the particular specification, W_i represents the weighting function, P_s the specified performance value and P_r the realized performance value. The three different types of specification are:

- constraints (inequalities) which must be satisfied. Their contribution to the error function is evaluated as $\varepsilon_{cs} = W_i|\frac{P_s-P_r}{P_s}|$ while the constraint is unsatisfied, $\varepsilon_{cs} = 0$ otherwise.
- costs to be minimized. Here $\varepsilon_{ct} = \pm W_i\frac{P_s-P_r}{P_s}$ depending on the type of the cost (maximize or minimize).
- conditions (equalities) which represent fixed points with tolerances. If the real value is outside the tolerances, then $\varepsilon_{cd} = W_i|\frac{P_s-P_r}{P_s}|$, $\varepsilon_{cd} = 0$ otherwise.

The overall function is the sum of the individual error functions pertaining to each specification. As an example, consider the optimization of a fast-inverter with the specifications shown in fig. 3, where A_v is the voltage gain, R_o is the output resistance, Pwr is the quiescent power, V_o is the quiescent output voltage and F_i is a formulation of Kirchoff's

example of specification set	
A_v	$maximize, 7$
$R_o(K\Omega)$	$\leq 1K$
$Pwr(mW)$	$\leq 4.5m$
F_i	$= 1.0$
$V_o(V)$	$= 0.5$

Fig. 3. Fast-inverter specification

current law represented by $F_i = |Ids_{Mn}/Ids_{Mp}|$. The notation ε_c means $\varepsilon_c(W_i, P_s, P_r, ST)$ where ST being the specification type. The total error of this optimization problem is :

$$\varepsilon_t = \varepsilon_{ct}(A_v) + \varepsilon_{cs}(R_o) + \varepsilon_{cs}(Pwr) + \varepsilon_{cd}(F_i) + \varepsilon_{cd}(V_o) \quad (2)$$

Once the error function has been created, each performance criterion must be evaluated and compared to its specified value. To evaluate each performance criterion, the user creates a simulation harness object which represents the various elements necessary to one simulation: the simulator command, options and analysis type, the harness file, and the post-simulation function to be applied. The harness file is created from a raw netlist, whereby it includes at run time the topology netlist and the design parameter values. It should be noted that for topologies belonging to the same category, the simulation harness for a given performance criterion is the same. Only the topology instance changes in the final netlist, as shown in fig. 4.

The post-simulation function translates the simulation results file into the performance to be calculated. A library of performance evaluation functions has been created, each operating on input and output signals, and some requiring certain accuracy control arguments.

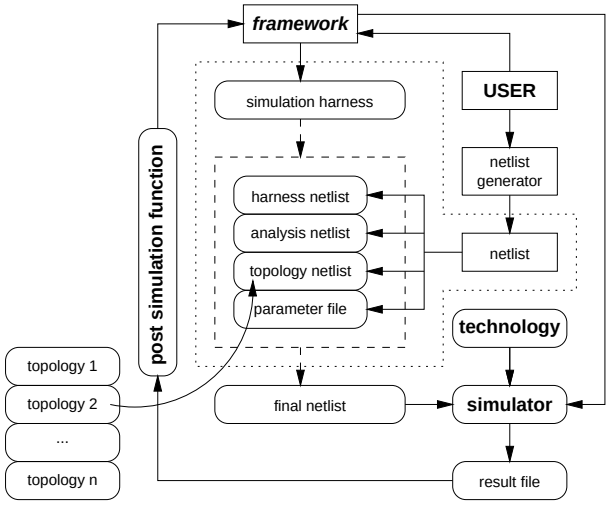


Fig. 4. Simulation harness and interface

The *topology*, a key element in the platform, is comprised of several elements (fig. 2(b)):

- synthesis information for specific design methods (an explicit procedure or heuristics, for example).
- objective performance indicators, which can be:
  - either a system of evaluation equations, formulated in terms of the physical dimensions of the topology,
  - or a link to a numerical simulation harness common to all topologies of one type (*category*), instantiating the topology under certain test conditions and targeting specific analyses.

  For each performance criterion, the user can capture an analytical equation in C-like code as well as various heuristics. A corresponding evaluation class is created and compiled, an instance of which can subsequently be dynamically loaded and used in each evaluation loop.
- individual dimensions: two types are used here, since we make an essential distinction between *abstract* and *physical* dimensions. The former represent the independent design variables that can be extracted from a formal representation of the optimization problem, while the latter are derived (usually explicitly) from the abstract dimensions for evaluation purposes. For example, a CMOS transistor is usually sized (abstract dimensions) by length and W/L ratio to distinguish influences on intrinsic gain and output conductance; whereas for evaluation purposes (physical dimensions) the absolute width and length values are calculated explicitly from the abstract dimension values.

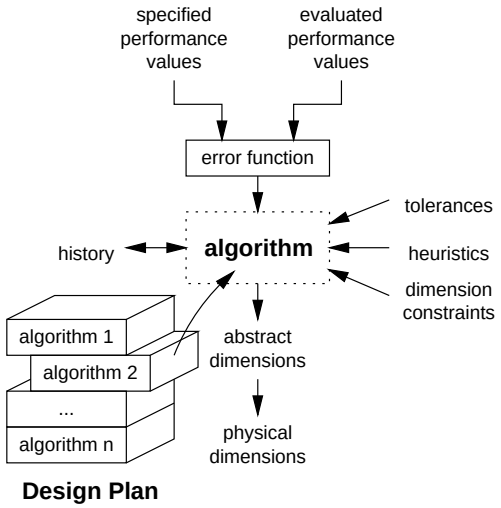


Fig. 5. Design plan concept

B. Design Plan

The manner in which the elements in the topology IP are exploited during the design process is formalized by a *design plan*, representing a sequence or a loop of sizing methods. The capability of drawing on a library of homogenized algorithms to build a large range of design plans is attractive, since the user can tailor the plan to the application without having to worry about low-level algorithm code details.

Fig. 5 shows what happens between performance evaluation for one set of dimensions, and generation of the following set. The error function is computed from specified

and evaluated performance values, as previously described. The current algorithm in the design plan stack is called for a method "hit" (one iteration) based on the algorithm's tolerances, design history and constraints and (according to user needs) heuristics. A new set of abstract dimensions is generated and translated into physical dimensions for evaluation.

III. Photoreceiver design methodology

We now present the implementation of our design methodology for the design of high-speed CMOS photoreceivers based on a PIN photodiode and transimpedance structure (fig. 6)[3]. The PIN photodiode is exposed to a light source of wavelength λ and optical power P_o, and generates a current I_{ph} according to its photoresponsivity R_d. The role of the transimpedance amplifier (TIA) is to convert the photocurrent to a voltage V_o, the whole operating at data rate D. We have used relatively simple blocks in order to demonstrate the feasibility of synthesis of the photoreceiver.

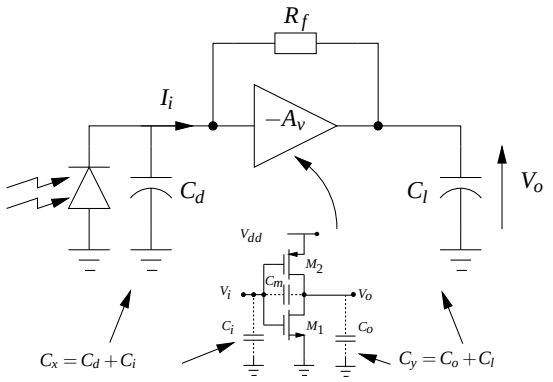


Fig. 6. Photoreceiver structure and equivalent transimpedance model.

The design methodology for the photoreceiver is based on three principal ideas. The first is to decompose the photoreceiver system into blocks based on their type and circuit structure complexity. The flow model shown in fig. 7 uses four blocks at three hierarchical levels. Each block specification holds information related to its design and evaluation as described in section II. The second idea is to define, for each block, procedural design methodologies, taking into account their respective positions in the hierarchy. The third idea is to develop a sizing methodology for each block at one hierarchical level, to verify that specified performance criteria are attained for all blocks at a given level. We will detail this further in this section.

It should be pointed out that our design objectives were (i) to maximize the bandwidth and minimize the power dissipation, and (ii) use the fixed structures defined in fig.6 (resistive feedback TIA). These objectives are sufficient to define the design problem completely and enable the explicit calculation of the dimensions of the structure. For this reason, the noise has not been considered as an objective in the design problem, although there is no reason why it could not handled with the described multi-domain synthesis approach.

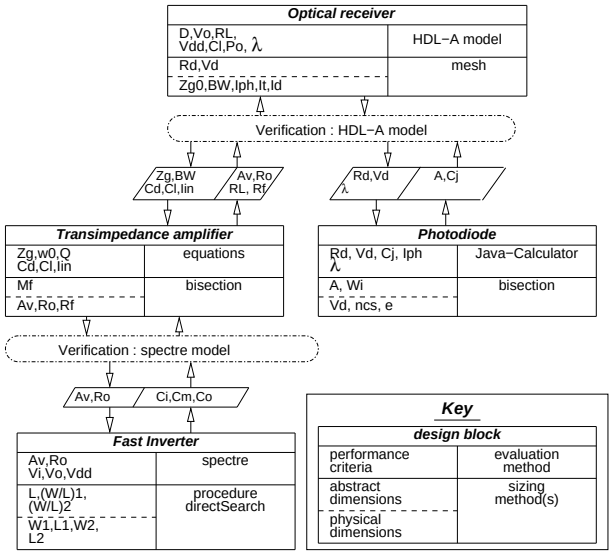


Fig. 7. Flow model for receiver synthesis.

A. Optical receiver

At this level we represent the optical receiver with electrical models [1], regardless of the physical structure of the photodiode. For this reason we have used an equivalent electrical model such as that used in Spice [4]. The specifications used at this level are the data rate D, optical input power P_o, wavelength λ, supply voltage V_{dd} and load capacitance C_l. The design parameters concern the photodiode (responsivity R_d, bias voltage V_d, -3db frequency f_c of the PIN photodiode and diode capacitance C_j) and the TIA (operating voltages V_i, V_o, V_{dd}, transimpedance gain Z_g and electrical bandwidth BW_e). In order to calculate the photo-current, we require the time constant τ_{opt}, which is an average of two phenomena (drift and diffusion) (equation 3).

$$\tau_{opt}^2 = \tau_{diff}^2 + \tau_{drift}^2 \Rightarrow \tau_{opt} = \sqrt{\tau_r^2 - \tau_{RC}^2} \qquad (3)$$

where the expression for the rise time τ_r and the time constant τ_{RC} is shown in fig. 8(a).

The junction capacitance C_j of the PIN photodiode is calculated by an approximate expression used in the Spice model (equation 4). This depends on the diode bias voltage V_d, the relative capacitance value at zero bias voltage $C_j(0)$, an empirical factor m and built-in voltage Φ_{bi} (this value depends on the wavelength).

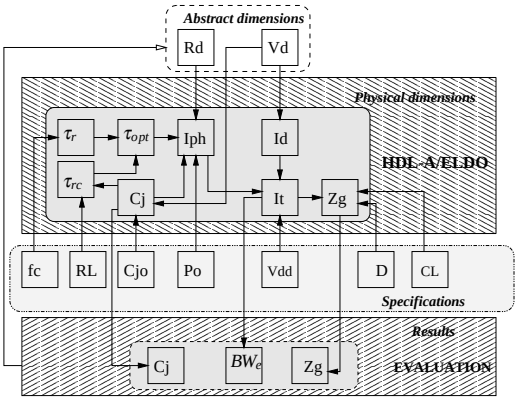
$$\begin{cases} C_j = C_j(0)(1-\beta\frac{V_d}{\Phi_{bi}})^{-m} \text{ si } V_d \leq 0 \\ \\ C_j = C_j(0)(1-\beta m\frac{V_d}{\Phi_{bi}}) \text{ si } V_d > 0 \end{cases} \qquad (4)$$

The system of equations used for the photoreceiver is shown in fig. 8(a) where R_s is the intrinsic series resistance, R_{shunt} is the shunt resistance and I_d is the current of the ideal diode. This system was implemented in an HDL-A[1] behavioral model, and was validated at both static and dynamic levels with experimental measurements of high-speed InGaAs photodiodes from Hamamatsu, giving an error of less than 5% [5].

[1] Analog hardware description language

Electrical PIN model
$I_{tot} = I_d + I_j + I_{shunt} - I_{photo}$
$I_{shunt} = \frac{V_d}{R_{shunt}}$
$I_j = C_d \frac{dV_d}{dt}$
$I_d = I_{sat}\left(e^{\frac{qV_d}{n_{ideal}}kT} - 1\right)$
$\tau_{RC} = R_L * C_j$
$\tau_r = \frac{0.35}{f_c}$
$R_d P_o = I_{photo} + \frac{\tau_{opt}}{2.2}\frac{dI_{photo}}{dt}$
$V = V_d + R_s I_t$

(a) System of equations for photodiode electrical model



(b) Optical receiver sizing

Fig. 8. High-level design procedure for optical receiver

The behavioral model of the TIA is, at this level, a simple linear first-order transfer function :

$$v_{out} = \frac{Z_g}{1 + \frac{s}{2\pi BW_e}} v_{in} \tag{5}$$

The input impedance of the TIA is simulated by the load resistance R_L. At the beginning of the sizing process, its value is estimated according to TIA specification parameters ($Z_{in} \approx R_f / A_v$). During later iterations, its value is extracted directly from transistor level simulations.

Both behavioral HDL-A models are included in an Eldo netlist, in which the simulation harness is also described. Care must be taken to constrain the sizing problem correctly: for example, taking too small a limit for the photodiode reverse bias voltage will result in over-constraint and the process will not converge; but too high a limit will place severe constraints on the operating region of the photodiode. We constrained $V_d < 2V_{dd}$, supposing separate supply voltages to the TIA and photodiode.

The sizing methodology is based on a direct search optimization algorithm [6], for which an explicit procedure for starting point generation is required. In this case, the initial value of responsivity is fixed at the maximum to extract a sufficient photocurrent I_{ph}; for bias voltage V_d we extract it value by equation (fig.8(a)) $V_d = V + R_s I_{ph}$ where $I_{ph} = R_d P_o$ and $V = V_{dd}/2$.

The local step search is as follows (fig. 9):

1. starting from the current point, X^n, apply fixed increments to each of the m variables. The user-defined increment ΔX, is first added to X_m^n,
2. if ε is not reduced, ΔX is subtracted from X_m^n,
3. if ε still not reduced, X_m^n is restored to its original value.
4. providing that at least one variable is successfully incremented, a new better point X^{n+1} will have been found: this becomes the new base point.
5. following a successful exploratory move, perform a pattern move by stepping along the line connecting the new X^n and X^{n+1}, the new computed point is X^{n+2}.
6. if no variable is successfully incremented, the increment ΔX is too large and so is reduced according to the user-defined scale factor.
7. termination of the algorithm search is controlled by max. number of iterations

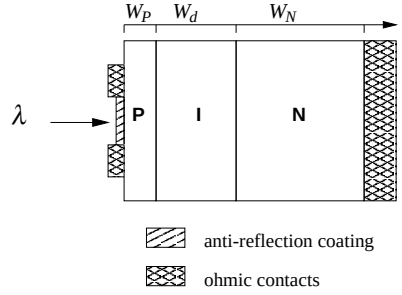
```
BEGIN
 n = 0 (iteration number)
 ε0 = ε(X)
 WHILE (n < NMAX)
 (NMAX: max.no of iterations)
 m = 0 (dimension number)
    WHILE (m < MMAX)
     (MMAX: max.no of dimensions)
       X_m^test = X_m^n + ΔX
          IF ε(X^test) > ε0
             X_m^test = X_m^n − ΔX
                IF ε(X^test) > ε0
                   X_m^(n+1) = X_m^n
                ELSE
                   X_m^(n+1) = X_m^test
                END IF
          ELSE
                   X_m^(n+1) = X_m^test
          END IF
       m++
    X^(n+2) = 2X^(n+1) − X^n
     n++
END
```

Fig. 9. Direct search algorithm

Cycle evaluation is shown in fig. 8(b). The performance criteria values are extracted directly throught the use of a function library for processing the results file of electrical simulations. Where the simulation using the behavioral models carries out a frequential analysis, the optical signal is modeled by a voltage source with amplitude equal to that of injected optical power. Bandwidth is extracted at -3dB using the post-processing function library, and extrapolated to the data rate using $D \approx 1.4BW$ to retrieve sufficient signal power above the fundamental. The block parameters are transmitted from the platform to the simulator. The evaluation cycle is based on total error calculation as explained in section A. The CPU time depends directly on the tolerance precision.

B. PIN photodiode

In order to evaluate the photodiode performance during the physical sizing process, we used an internally developed calculator which is based on standard PIN photodiode equations from the literature, shown in fig. 11(a) [7, 8]. The physical structure of the PIN photodiode is shown in fig. 10(a).



(a) Physical structure of PIN photodiode

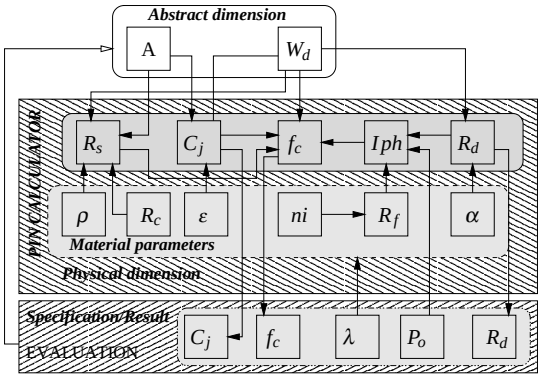
Material parameters of InGaAs techmology		
α	absorption coefficient	$1e+4\ (cm^{-1})$
ε	permittivity	13.2
ni	reflexion factor	3.5
R_c	contact resistance	$20\ (\Omega)$
ρ	charge density	$10e+6(\Omega cm^2)$

(b) Material parameters of InGaAs technology

Fig. 10. Physical representation of PIN photodiode

System equation of PIN calculator
$R_d = 1 - \frac{1}{exp(\alpha\ w_d)}$
$C_j = \frac{\varepsilon\ A}{w_d}$
$R_f = (\frac{ni-1}{ni+1})^2$
$Iph = \frac{(1-R_f)\ R_d\ Po\ e}{h\ \nu}$
$fc = \sqrt{\frac{(Iph\ R_j)^2+1}{2\pi Cj\ R_j}}$
$R_s = \frac{w_s - w_d}{A}\ \rho + R_c$

(a) System of equations of PIN calculator



(b) Design procedure for PIN photodiode

Fig. 11. Evaluation and design flow for PIN photodiode

At this level, the specifications are the photoresponsivity R_d, junction capacitance C_j, photocurrent I_{ph}, wavelength λ, cutoff frequency f_c, and series resistance R_s. We also define material parameters such as energy gap, average carrier mobility, absorption coefficient α at the required wavelength as shown in fig. 10(b). The value of α is fixed in this work since λ is known. To enable a choice of wavelengths, α should be a table of values. R_j represents a parallel resistor, which models the reverse, leakage, or dark current of the photodiode. It is usually very large and can be neglected in most cases. The value of R_j in our case is fixed at $20G\Omega$.The abstract dimensions to be used in the sizing process represent the diode structure: width of intrinsic zone thickness w_d, area A.

The sizing procedure of the photodiode is again based on a direct search optimization algorithm. In this case, the initial value of w_d is calculate by $w_d = log(1-R_d)/\alpha$ and $A = C_j w_d/\varepsilon$. Fig. 11(b) shows the interdependency between abstract and physical dimensions, specifications and material parameters.

The choice of wavelength influences the choice of semiconductor material, for which the absorption coefficient is the essential parameter. The maximum value for detectable wavelength for a material of know bandgap energy E_g is:

$$\lambda < \frac{1240}{E_g} \tag{6}$$

In our case we have used InGaAs semiconductor material for which the bandgap energy value is 1.424 eV, and the value of λ is limited to 0.8-0.87 μm.

C. TIA

The basic transimpedance amplifier structure in a typical configuration was shown in fig. 6. We target CMOS technology and as such we can replace the amplifier block by a model with capacitive input impedance.

The complete circuit model that we use for this first analysis is shown in fig. 12 (note that we model the photodiode simply as a current source with parasitic capacitance).

The expression for the transimpedance gain Z_g is then:

$$Z_g(s) = \frac{v_o}{i_i} = \frac{Z_{g0} + a_1 s}{1 + b_1 s + b_2 s^2} \tag{7}$$

where:

$$Z_{g0} = \frac{R_o - R_f A_v}{1 + A_v}$$
$$a_1 = \frac{C_m R_o}{1 + A_v}$$
$$b_1 = \frac{C_x(R_o + R_f) + C_y R_o + C_m R_f (1 + A_v)}{1 + A_v} = \frac{1}{\omega_0 Q}$$
$$b_2 = \frac{R_o R_f (C_x C_y + C_x C_m + C_y C_m)}{1 + A_v} = \frac{1}{\omega_0^2}$$

In these expressions, $C_x = C_d + C_i$ and $C_y = C_l + C_o$. The system described in (7) is one of second order. By identification, and introducing the multiplying factors $M_f = R_f/R_o$, $M_x = C_x/C_y$ and $M_m = C_m/C_y$, we have expressions for pole angular frequency ω_0 and quality factor Q as shown in equations (8,9).

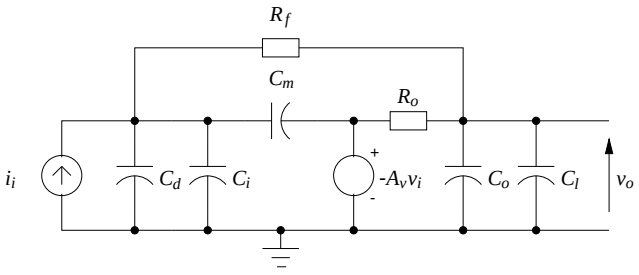


Fig. 12. Equivalent transimpedance model.

$$\omega_0 = \frac{1}{R_o C_y}\sqrt{\frac{1+A_v}{M_f(M_x+M_m+M_xM_m)}} \tag{8}$$

$$Q = \frac{\sqrt{M_f(M_x+M_m(1+M_x))(1+A_v)}}{1+M_x(1+M_f)+M_mM_f(1+A_v)} \tag{9}$$

Note that in our work we have neglected the effect of the zero caused by the Miller capacitance C_m.This assumption is true as long as

$$A_v > \frac{M_m^2}{M_f(M_x+M_m+M_xM_m)} - 1 \tag{10}$$

which is likely to be valid if the Miller capacitance is merely the parasitic gate-drain capacitance in the internal amplifier[9]. Sizing is iterative using a simple bisection algorithm [10], including a boundary detection and extension mechanism (fig. 14). This application converged systematically in under a second (typically a few tens of iterations) to a precision of better than 0.01% on a Sun Ultra 5 workstation. The desired TIA performance criteria (transimpedance

Vary M_f by bisection and calculate	
$A_v = \frac{a-2bcQ^2 \pm \sqrt{a^2-4abcQ^2}}{2c^2Q^2} - 1$	if $M_m \neq 0$
$A_v = \frac{b^2Q^2}{M_fM_x} - 1$	if $M_m = 0$
$R_o = \frac{\sqrt{\frac{1+A_v}{M_xM_f}}}{\omega_0 C_y}$	
$R_f = M_f R_o$	
$Z'_{g0} = \frac{R_o - R_f A_v}{1+A_v}$	
where: $a = M_f(M_x+M_m+M_xM_m)$	
$b = 1+M_x(1+M_f)$	
$c = M_mM_f$	
until $\lvert Z_{g0} - Z'_{g0}\rvert < \varepsilon$	

Fig. 13. System of equations used in design procedure for TIA

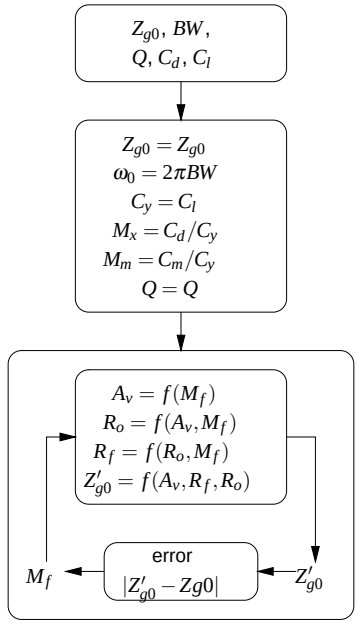


Fig. 14. Design procedure for TIA.

gain Z_g, bandwidth BW_e and quality factor Q) and operating conditions (photodiode capacitance C_d and load capacitance C_l) allow generation of component values for the feedback resistance R_f and the voltage amplifer (open loop gain A_v, output resistance R_o).

Taking into consideration the physical realization of the amplifier, those with requirements for low gain and high output resistance (high R_o/A_v ratio) are the easiest to build, and also require the least quiescent current and area. We have plotted this quantity against the transimpedance amplifier specifications (bandwidth and transimpedance gain) for $C_x = C_d = 500\,fF$ and $C_y = C_l = 100\,fF$ (fig. 15).

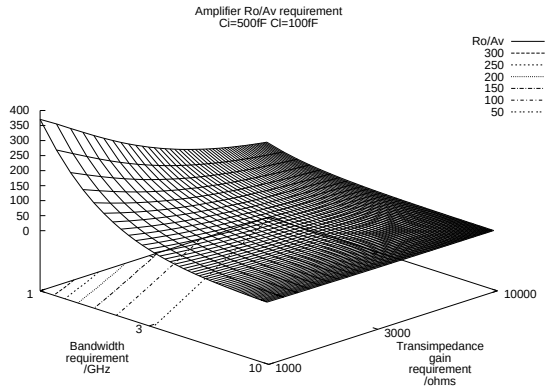


Fig. 15. Transimpedance design space for R_o/A_v requirements

D. Internal amplifier

At the physical level, we have used a simple inverter structure for the internal amplifier as shown in fig. 6. The specifications at this level are generated directly by the TIA block according to the overall design flow (fig.7). We have devel-

Internal Amplifier procedure

$$I_{ds_1} = \frac{1}{R_o\left(1+\frac{Vea_2}{Vea_1}\right)}$$

$$\frac{g_{m_1}}{I_{ds_1}} = \frac{A_v}{Vea_1 L_{min}} \frac{1+\frac{Vea_2}{Vea_1}}{1+\frac{(W/L)_2}{(W/L)_1}} \frac{V_{gs2}-V_{t2}}{V_{gs1}-V_{t1}}$$

$$\Delta_1 = \sqrt{\frac{KP_2(W/L)_2}{KP_1(W/L)_1}}$$

$$\Delta_2 = \frac{V_{dd}+Vth_2-Vgs_1}{Vgs_1-Vth_1}$$

Fig. 16. System of equations of design procedure for internal amplifier

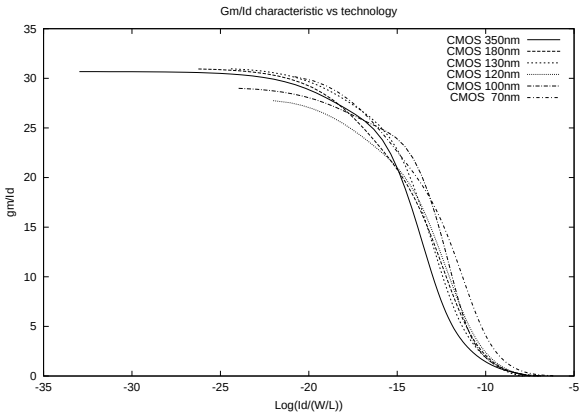


Fig. 17. gm/Id caracteristics vs log(Id/(W/L)

oped a procedure to make a first-cut sizing of the inverter based on the transcanductance to current g_m/I_D methodology [11], enabling us to simplify the design problem without losing accuracy.

In practice, the range of values of g_m/I_d is limited to 30 V^{-1}. It is a characteristic common to all the transistors of the same type (nMOS or pMOS) resulting from the same manufacturing technology. Fig. 17 presents g_m/I_d characteristics nodes versus $log(I_d/(W/L))$ for various technology nodes (Berkeley predictive model parameters) [12], where W/L is the transistor size ratio.

The specifications at this level are static gain A_v, output resistance R_o and supply voltage. The procedure used for sizing the internal amplifier is shown in fig. 16, where the value of parameter Δ_1 represents a ratio between the sizes of M_1 and M_2. The value of Δ_1 is determinated by a saturation condition represented by Δ_2.

The procedure consists of calculating a value of $(g_m/I_d)_1$ by the expression shown in fig. 16, and then extracting the corresponding value of $log(Id_1/(W/L)_1)$. The value of the current I_{d_1} calculated by the expression shown in fig. 16, gives the value of the size of transistor M_1. This procedure is followed by a direct search optimization algorithm for fine-tuning. The parasitic capacitances are extracted at the TIA level for use in the TIA sizing procedure. V_{ea} represents the Early voltage which depends on the channel length modulation parameter.

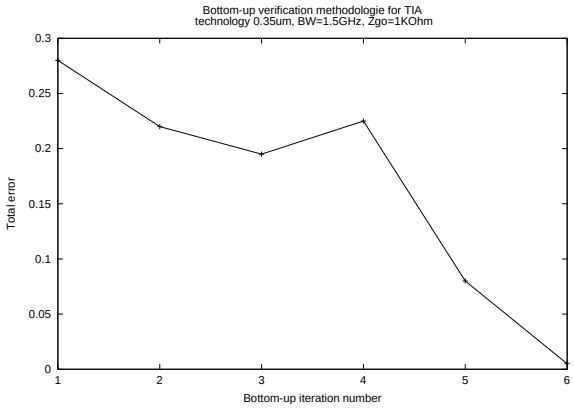


Fig. 18. Automated verification iterations for TIA optimization.

IV. Automated verification

In this section we define the methodology used for automating the specification verification and correction shown in fig. 7. This is based on the simulation of the complete netlist representing all blocks in one level, from which the various parameters needed for this operation are extracted from the lower level. The correction of the specification is achieved by the following equation, applied to each performance criterion:

$$S_{corr} = S_{old} \pm \Delta \tag{11}$$

where $\Delta = P_{req} - P_{sim}$ and P_{req} represents the performance requirement reached by behavioral model simulation during the top-down phase; P_{sim} represents the simulated performance value generated during the bottom-up verification phase; S_{old} is the specification corresponding to the performance requirement (P_{req}); and S_{corr} is the corrected specification value to be used in a new sizing process. In the flow model for receiver synthesis shown in fig. 7 we have two verification stages, detailed in the following paragraphs:

A. TIA

The verification of the TIA is based on simulation of the complete netlist with $Spectre^{TM}$. The physical transistor dimensions are extracted directly before the optimization of the inverter, as shown in fig. 7. If the verification at this stage shows that all specifications are satisfied, the bottom-up flow continues up to the next level. Otherwise the specifications for the TIA gain and bandwidth are corrected, the new capacitance values C_i, C_m,C_o are extracted by the library function and a new evaluation of the TIA begins. Fig. 18 shows the efficiency of this approach in progressively decreasing the total verification error during TIA optimization.

B. Optical receiver

Optical receiver performance verification and correction is achieved by the simulation of the complete netlist representing the HDL-A photodiode model and the TIA structure with an electrical simulator. The physical transistor dimensions representing the inverter are extracted directly before the optimization of the TIA has finished. For the photodiode, we extracted the final value of performance.

V. RESULTS

The optimization aim is to minimize the value of the overall error function. To explain this, we have optimized a fast inverter where a diode transistor M_3 is added at the output node to increase bandwidth. In the case where $\varepsilon_x = \varepsilon_{cs}$ the ideal solution is $\varepsilon_t = 0$, and in the other case, where the cost specification for the gain ($\varepsilon_x = \varepsilon_{ct}$) is used (fig. 19(a)), the solution is obtained for negative values of ε_t. For F_i we have shown a condition specification since the significant interval value is more restricted around one value. We have used a direct search algorithm (Hooke and Jeeves) to resolve this example.

The reduction in total error with the number of loop iterations in both cases is shown in fig. 20(a) and fig. 20(b), and the optimised result in fig. 19(b) and fig. 19(c).

Using this methodology and predictive BSIM3v3 and BSIM4 models for technology nodes from 350nm down to 45nm [12], we also generated design parameters for 1THzΩ

	$Spec.set1$	$Spec.set2$
A_v	≥ 7	$maximize, 7$
$R_o(K\Omega)$	$\leq 1K$	$\leq 1K$
$Pwr(mW)$	$\leq 4.5m$	$\leq 4.5m$
F_i	$= 1.0$	$= 1.0$
$V_o(V)$	$= 0.5$	$= 0.5$

(a) Fast-inverter specification

$Set1 : error function$		$Result$
A_v	$\varepsilon_{cs}(1,7,P_r,\geq)$	7.32
$R_o(K\Omega)$	$\varepsilon_{cs}(1,1K,P_r,\leq)$	0.221K
$Pwr(mW)$	$\varepsilon_{cs}(1,4.5m,P_r,\leq)$	4.308m
F_i	$\varepsilon_{cd}(10,1,P_r,=)$	1.005
$V_o(V)$	$\varepsilon_{cd}(1,0.5,P_r,=)$	0.472

(b) Fast-inverter result of spec. set1

$Set2 : error function$		$Result$
A_v	$\varepsilon_{ct}(1,7,P_r,maximize)$	14.462
$R_o(K\Omega)$	$\varepsilon_{cs}(1,1K,P_r,\leq)$	0.360K
$Pwr(mW)$	$\varepsilon_{cs}(1,4.5m,P_r,\leq)$	6.238m
F_i	$\varepsilon_{cd}(10,1,P_r,=)$	1.617
$V_o(V)$	$\varepsilon_{cd}(1,0.5,P_r,=)$	0.562

(c) Fast-inverter result of spec. set2

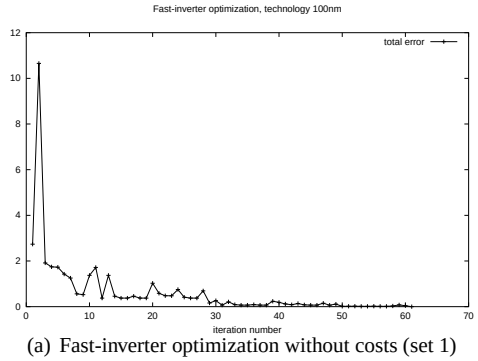
Fig. 19. Fast-inverter specification and optimised result

TIAs to evaluate the evolution in critical characteristics with technology node. Fig. 21 shows the results of transistor level simulation of fully generated TIA circuits at each technology node.

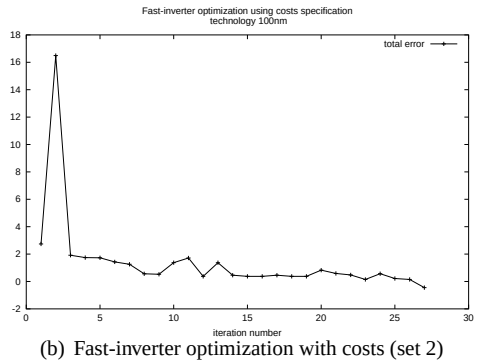
According to traditional *"shrink"* predictions, which consider the effect of applying a unitless scale factor of $1/k$ to the geometry of MOS transistors, the quiescent power and device area should decrease with $1/k^2$ factor.

Between 180nm and 70nm technology nodes $k^2 \simeq 6.61$, which is verified through our sizing optimization procedure. With this methodology we can also find a particular specification to a given tolerance, as shown in fig. 22.

With a predictive BSIM4 model for the 45 nm technology node, we have plotted the active area of the generated



(a) Fast-inverter optimization without costs (set 1)



(b) Fast-inverter optimization with costs (set 2)

Fig. 20. Fast-inverter optimization

TIA with static power dissipation for bandwidths 1GHz to 5GHz with Zg at 1kΩ and the quality factor Q at $1/\sqrt{2}$. We have also designed a TIA with BSIM3v3 models for a 0.35um technology using low tolerance specifications shown in fig. 23(a). The specification $Q = 1/\sqrt{2}$ allows a maximum bandwidth/power ratio, and V_i and V_o are specified as $V_{dd}/2$ allowing maximum gain for the internal amplifier. The optimization result and characteristics are shown in fig. 23(b). Finally as an example of the type of validation of the described approach, the method was used to design a 0.13μm CMOS $1THz\Omega$ TIA with an InGaAs PIN photodiode. The simulated photoreceiver performance is summarized in table I.

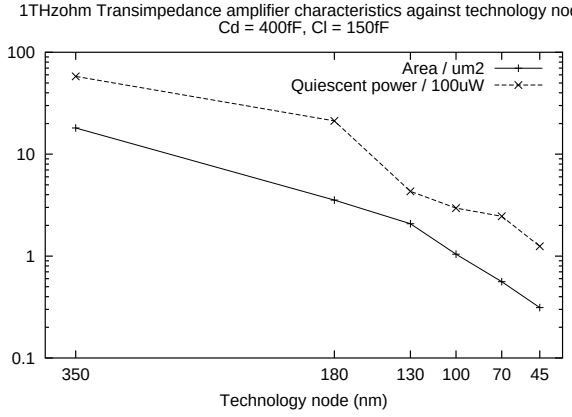


Fig. 21. Transimpedance characteristics vs technology node

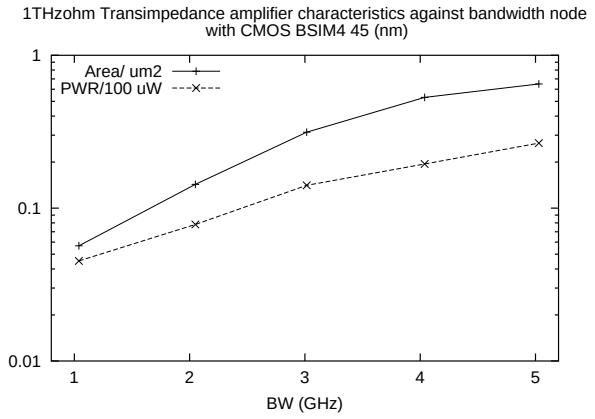


Fig. 22. Transimpedance characteristics vs bandwidth node with 45nm technology.

Condition		Specification	Tolerance	Result
technology (nm)	350	BW_e (GHz)= 1.5	0.05%	1.473
$V_{dd}(V)$	3.3	$Z_g(K\Omega) = 1$	0.02%	1.006
$C_l(fF)$	150	pwr (mW)	–	6.12
$C_d(fF)$	400	C_m (fF)	–	17.43
$I_d(uA)$	50	C_i (fF)	–	45.503
		$R_f(K\Omega)$	–	1.406
		$V_i(V)$= 1.65	0.05%	1.58
		$V_o(V)$= 1.65	0.02%	1.62
		Q $= 1/\sqrt{2}$	0.004%	0.7045

(a) Transimpedance specification and result

Transistor size	
All transistor L (um)	0.35
W(M1)/L	72
W(M2)/L	144

CPU Characteristic	
time	30 mn
Bottom-Up loop number	6
$Spectre^{TM}$simulation number	265

(b) Transistor sizing result and CPU characteristics

Fig. 23. Optimization characteristics and results of 0.35 um CMOS TIA design

VI. Conclusion

We have presented the implementation of a complete hierarchical synthesis methodology for high-speed photoreceiver front-ends. We have developed a method of communicating between different hierarchical levels based on such models. With it we can size heterogeneous systems and generate complete dimension sets for precise specifications in short synthesis times. The accurate results of this methodology have been used in the context of comparing power requirements for integrated electrical and optical links.

TABLE I
Simulated performance of photoreceiver.

Parameter	Value
Optical power P_{opt}	*50 μW*
Wavelength λ	*850nm*
Bandwidth BW	*1.1 GHz*
Junction capacitance C_j	*94.1 fF*
Photocurrent I_{ph}	*42.3 μA*
Photodiode reverse bias voltage V_d	*1.87 V*
Intrinsic zone thickness d	*10 μm*
Photodiode responsivity R	*0.85 A/W*
Transimpedance gain Z_{g0}	*62.6 db*
M_1 *transistor width* W_1	*90.4 μm*
M_2 *transistor width* W_2	*4.2 μm*
M_3 *transistor width* W_3	*2.7 μm*
M_{1-3} *transistor lengths L*	*0.13 μm*
Transimpedance feedback resistance R_f	*1.5 k Ω*
Supply voltage V_{dd}	*1.2V*
Load capacitance C_l	*6.47fF*
DC input voltage V_{in}	*0.7 V*
DC output voltage V_{out}	*0.6 V*
Quiescent power	*4.2 mW*

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