Design methodologies for high-speed CMOS photoreceiver front-ends

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Abstract

A hierarchical design methodology for wide bandwidth photoreceiver front-ends is presented in this paper. We propose a unified approach for both optoelectronic and electronic components in the front-end, capable of improving system performance with respect to traditional segregated design flows. Based on a synthesis platform aimed at fast multi-domain system design automation, we optimize photodiode structure and CMOS transimpedance amplifiers for different technology nodes with accurate performance prediction.

1. Introduction

The rapid development of telecommunication services has engendered needs for low cost solutions with operating frequencies in the Giga-Hertz range. Optical communication systems provide these services for both short and long distances. Thanks to the monolithic integration of optical and electronic components, in OEICs (**O**pto**E**lectronic **I**ntegrated **C**ircuit), superior performance can be achieved with significant cost reduction.

A typical optical link is composed of three components [1]:

(i) the transmitter, which converts the electrical signal to an optical one;

(ii) the transmission medium, representing waveguide, fiber or free space between components;

(iii) the receiver with which we receive the optical signal and convert it back to an electrical one.

Of these, the receiver is the part that presents the greatest limit to high-speed performance. It is composed of several functional blocks; in this work, we focus on the photoreceiver front-end. Sizing of such blocks is a problem representative of many for which existing design technology is inadequate due to their *complexity* and *heterogeneity*. Concerning the complexity, a simple photoreceiver can be implemented with a minimum of two blocks. At high frequencies we need to take all parameters into account, and consequently the set of design parameters increases. Efficient evaluation of these circuits is increasingly difficult and requires long CPU times.

Generally, sizing at transistor level becomes prohibitive above a certain number of transistors since the number of design parameters, N, is of the same order of magnitude as the number of transistors in the block. If the number of solutions visited for each individual design parameter is represented by s, the time necessary for each evaluation carried out during the design process by T_e, and the parameter generation time by t_g, then the total design time t_d is:

$$t_d = (T_e + t_g) \prod_{i=1}^{N} s_i$$

which is clearly impractical for large blocks. For this reason, we must use techniques to simplify the design problem and reduce its complexity; design tools capable of handling design problems through several hierarchical loops are therefore necessary. As concerns heterogeneity, the photoreceiver contain two components of different physical type, a photodiode (optical type) and a transimpedance amplifier (electrical type). For synthesis, this is the greatest problem, since no existing tool is capable of taking heterogeneity into consideration, meaning in our case that the OEIC system is not optimized and the design process inefficient.

Our solution addresses both problems and consists of (i) carrying out a top-down design space exploration using behavioral models to the physical level, (ii) physical sizing linking directly from a co-synthesis backplane to the various evaluation tools, as shown in figure 1, and (iii) subsequent bottom-up design verification using model parameter extraction. Our methodology has been completely integrated in an in-house synthesis platform. In this paper we

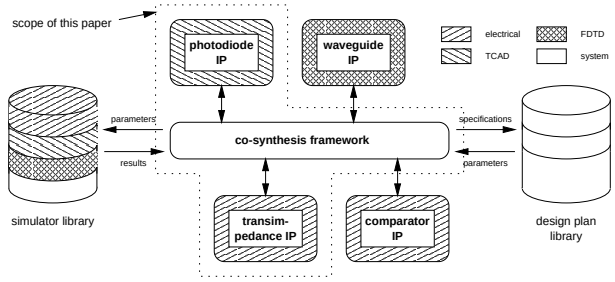


Figure 1. Cosynthesis backplane showing multiple simulators and design plans.

present the methodology applied to the photoreceiver. In section 2, we present the sizing procedure for each individual block including a global automated verification stage. We present the results of our work in section 3.

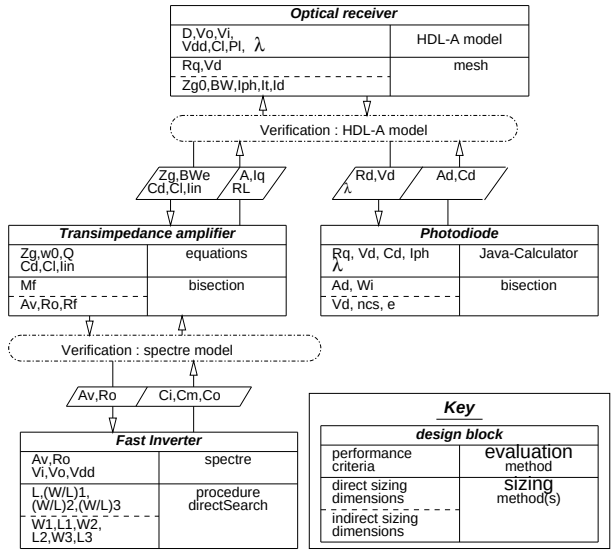


Figure 2. Flow model for receiver synthesis.

2. Photoreceiver design methodology

We now present the implementation of a design methodology for the design of high-speed CMOS photoreceivers based on a PIN photodiode and transimpedance structure. The PIN photodiode is exposed to a light source of wavelength λ and optical power P_o, and generates a current I_{ph} according to its photoresponsivity R_q. The role of the transimpedance amplifier (TIA) is to convert the photocurrent to a voltage V_o, the whole operating at data rate D. We have used relatively simple blocks in order to demonstrate the feasibility of synthesis of the photoreceiver.

The design methodology for the photoreceiver is based on three principal ideas. The first is to decompose the photoreceiver system into blocks based on their type and circuit structure complexity. The flow model shown in figure 2 uses four blocks at three hierarchical levels. The second idea is to define for each block procedural design methodologies, taking into account their respective positions in the hierarchy. The third idea is to develop a sizing methodology for each block at one hierarchical level, to verify that specified performance criteria are attained for all blocks at a given level. We will detail this further in this section.

2.1 Optical receiver

At this level we represent the optical receiver with electrical models [1], regardless of the physical structure of the photodiode. For this reason we have used an equivalent electrical model such as that used in Spice [6]. The specifications used at this level are the data rate D, optical input power P_o, wavelength λ, supply voltage V_{dd} and load

System of equations of electrical PIN model

$$I_{tot} = I_d + I_j + I_{shunt} - I_{photo}$$

$$I_{shunt} = \frac{V_d}{R_{shunt}}$$

$$I_j = C_d \frac{dV_d}{dt}$$

$$I_d = I_{sat}\left(e^{\frac{qV_d}{n_{ideal}kT}} - 1\right)$$

$$R_q P_{opt} = I_{photo} + \frac{\tau_{opt}}{2.2}\frac{dI_{photo}}{dt}$$

$$V = V_d + R_s I_t$$

Figure 3. System of equations for photodiode electrical model.

capacitance C_l. The design parameters concern the photodiode (responsivity R_q, bias voltage V_d, optical bandwidth BW_{opt} and diode capacitance C_d) and the TIA (operating voltages V_i, V_o, V_{dd}, transimpedance gain Z_g and electrical bandwidth BW_e). We require the rise time τ_r in order to calculate the photodiode current, τ_r expressed (i) as the frequency f_c at which the photodiode output decreases by 3dB, and (ii) τ_{RC} the RC constant of the diode-circuit combination. The final system of equations used for the photoreceiver is shown in figure 3 where R_s is the intrinsic series resistance, R_{shunt} is the shunt resistance and I_d is the current of ideal diode. This system was implemented in an HDL-A behavioral model [7], and was validated at both static and

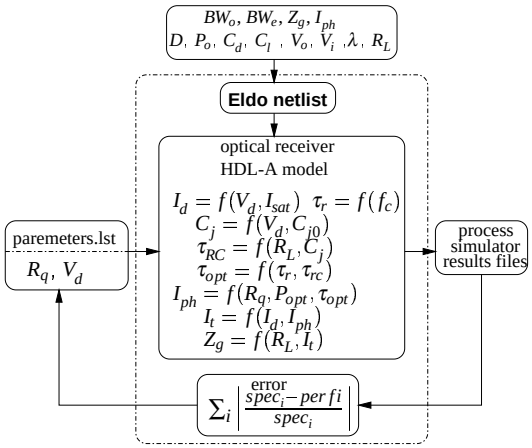


Figure 4. Optical receiver sizing.

dynamic levels with experimental measurements of high-speed InGaAs photodiodes from Hamamatsu [3]. The behavioural model of the TIA is, at this level, a simple linear transfer function :

$$v_{out} = \frac{Z_g}{1 + \frac{s}{2\pi BW_e}} v_{in}$$

Both behavioral HDL-A models are included in an Eldo netlist, in which the simulation harness is also described. Care must be taken to constrain the sizing problem correctly: for example, the photodiode reverse bias voltage as too small a limit will result in over-constraint and the process will not converge; but too high a limit will place severe constraints on the operating region of the photodiode. We constrained $V_d < 2V_{dd}$, supposing separate supply voltages to the TIA and photodiode.

The sizing methodology is based on a direct search optimization algorithm, for which we require a more explicit procedure for starting point generation. Cycle evaluation is shown in figure 4. The performance criteria values are extracted directly throught the use of a function library for processing the results file of Eldo simulations. Where the simulation using the behavioral models carries out a frequential analysis, the optical signal is modeled by a voltage source with amplitude equal to that of injected optical power. Bandwidth is extracted at -3dB using the post-processing function library, and extrapolated to the data rate using $D \approx 1.4BW$ to retrieve sufficient signal power above the fundamental. The block parameters are transmitted from the platform to the simulator through the file "parameters.lst", as shown in figure 4. The evaluation cycle is based on total error calculation as shown in figure 4, where $spec_i$ is the specification of performance $perf_i$. With this formulation of error, we can apply different tolerances for each specification. The CPU time depends directly on the tolerance precision.

2.2 PIN photodiode

In order to evaluate the photodiode performance during the physical sizing process, we used an internally developed calculator shown in figure 5, which is based on standard PIN photodiode equations from the literature [4]. At this

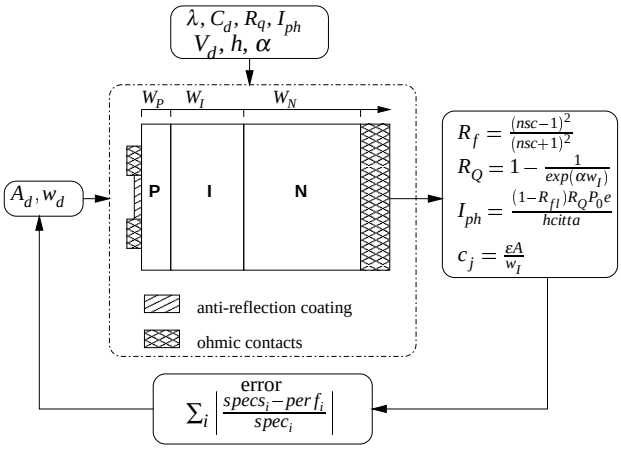


Figure 5. Theoretical equations and sizing method for photodiode.

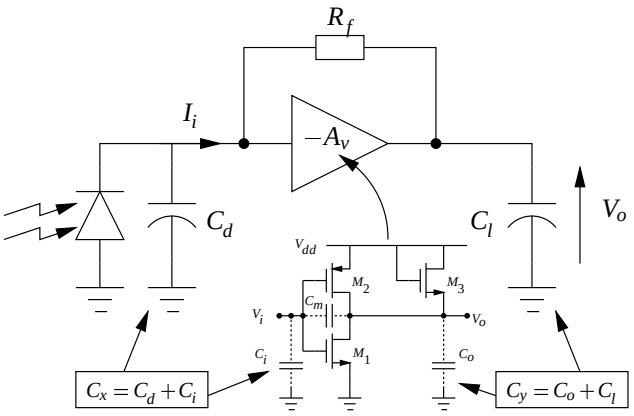
level, the specifications are the photoresponsivity R_q, junction capacitance C_d, photocurrent I_{ph}, wavelength λ, optical bandwidth BW_{opt}, reverse bias voltage V_d. We also define material parameters such as energy gap, absorption coefficient at required wavelength, average carrier mobility, etc. The physical dimensions to be used in the sizing process represent the diode structure: intrinsic zone thickness, area.

The sizing procedure of the photodiode is again based on a direct search optimization algorithm. The corresponding diagram is shown in figure 5. The design parameters are simply the physical dimensions of the structure, and the material composition of the PIN photodiode is determined by the interval of wavelength λ.

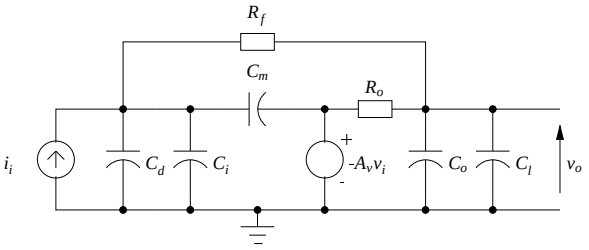
2.3 TIA

The basic transimpedance amplifier structure in a typical configuration is shown in figure 6(a) . We target CMOS technology and as such we can replace the amplifier block by a model with capacitive input impedance. The complete circuit model that we use for this first analysis is shown in figure 6(b) (note that we model the photodiode simply as a current source with parasitic capacitance[5]). The expression for the transimpedance gain Z_g is shown in equation (1) figure 7(c).

The system described (figure 7(c)) is one of second order. By identification, and introducing the multiplying factors $M_f = R_f/R_o$, $M_i = C_x/C_y$ and $M_m = C_m/C_y$, we have expressions for ω_0 and Q shown in (2,3) figure 7(c). Note that in our work we have neglected the effect of the zero caused by the Miller capacitance C_m.



(a) Photoreceiver front-end structure.



(b) Basic transimpedance circuit model.

Figure 6. Photoreceiver structure and equivalent transimpedance model.

This assumption is true as long as the condition shown at (4,5) (figure 7(c)) is valid [9]. Sizing is iterative using a simple bisection algorithm [10], including a boundary detection and extension mechanism (figure 8). This application converged systematically in under a second (typically a few tens of iterations) to a precision of better than 0.01% on a Sun Ultra 5 workstation. The desired TIA performance criteria (transimpedance gain Z_g, bandwidth BW_e and quality factor Q) and operating conditions (photodiode capacitance C_d and load capacitance C_l) allow generation of component values for the feedback resistance R_f and the voltage amplifer (open loop gain A_v, output resistance R_o).

Vary M_f by bisection and calculate
$A_v = \frac{a-2bcQ^2 \pm \sqrt{a^2-4abcQ^2}}{2c^2Q^2} - 1$ if $M_m \neq 0$
$A_v = \frac{b^2Q^2}{M_f M_x} - 1$ if $M_m = 0$
$R_o = \frac{\sqrt{\frac{1+A_v}{M_x M_f}}}{\omega_0 C_y}$
$R_f = M_f R_o$
$Z'_{g0} = \frac{R_o - R_f A_v}{1+A_v}$
where: $a = M_f(M_x + M_m + M_x M_m)$
$b = 1 + M_x(1+M_f)$
$c = M_m M_f$
until $\lvert Z_{g0} - Z'_{g0} \rvert < \varepsilon$

(a) Transimpedance sizing procedure.

First-cut sizing of the amplifier	
$V_{gst1} = V_i - V_{t1}$,	$V_{gst2} = V_i - V_{dd} - V_{t2}$
$g_{m1} = \frac{A_v/R_o}{\frac{V_{gst1}}{\lvert V_{gst2} \rvert}+1}$,	$\left(\frac{W}{L}\right)_1 = \frac{g_{m1}}{K_n V_{gst1}}$
$g_{m2} = g_{m1}\frac{V_{gst1}}{\lvert V_{gst2} \rvert}$,	$\left(\frac{W}{L}\right)_2 = \frac{g_{m2}}{K_p \lvert V_{gst2} \rvert}$
$L_{1,2,3} = L_{min}$,	$\left(\frac{W}{L}\right)_3 = \frac{W_{min}}{L_{min}}$

(b) Internal amplifier sizing procedure.

Theorical analysis equation
$Z_g(s) = \frac{v_o}{i_i} = \frac{Z_{g0} + a_1 s}{1 + b_1 s + b_2 s^2}$ (1)
$\omega_0 = \frac{1}{R_o C_y}\sqrt{\frac{1+A_v}{M_f(M_x+M_m+M_x M_m)}}$ (2)
$Q = \frac{\sqrt{M_f(M_x+M_m(1+M_x))(1+A_v)}}{1+M_x(1+M_f)+M_m M_f(1+A_v)}$ (3)
$A_v > \frac{M_m^2}{M_f(M_x+M_m+M_x M_m)} - 1$ (4)
$M_m \gg \frac{1}{2}(M_f(1+M_x) \pm \sqrt{\delta})$ (5)
$\delta = \sqrt{(M_f(1+M_x))^2 + 4M_f M_x}$

(c) Theorical equations and condition analysis of transimpedance.

Figure 7. Algorithms for transimpedance sizing.

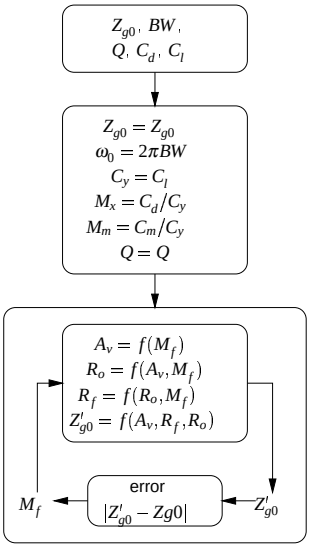


Figure 8. Design procedure for TIA.

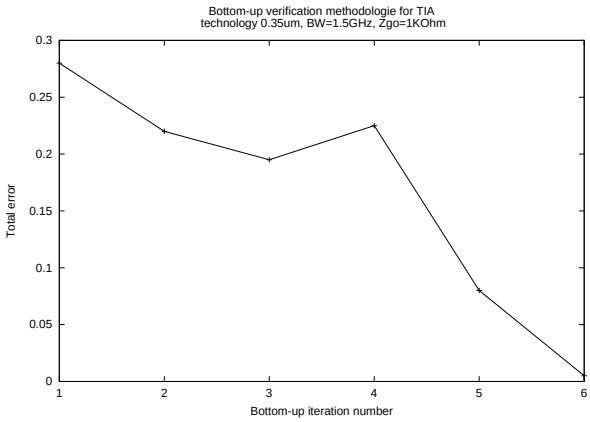


Figure 9. Automated verification iteration for TIA optimization.

2.4 Automated verification

In this section we define the methodology used for automating the specification verification and correction shown in figure 2. This is based on the simulation of the complete netlist representing all blocks in one level, from which the various parameters needed for this operation are extracted from the lower level. The correction of the specification is achieved by the following equation, applied to each performance criterion: $S_{corr} = S_{old} \pm \Delta$ where $\Delta = P_{req} - P_{sim}$ and P_{req} represents the performance requirement reached by behavioral model simulation during the top-down phase; P_{sim} represents the simulated performance value generated during the bottom-up verification phase; S_{old} is the specification corresponding to the performance requirement (P_{req}); and S_{corr} is the corrected specification value to be used in a new sizing process. In the flow model for the synthesis receiver shown in figure 2 we have two verification stages :

- the verification of the TIA is based on simulation of the complete netlist with $Spectre^{TM}$. The physical transistor dimensions are extracted directly before the optimization of the fast inverter, as shown in figure 2. If the verification at this stage shows that all specifications are satisfied, the bottom-up flow continues up to the next level. Otherwise the specifications for the TIA gain and bandwidth are corrected, the new values of capacitance C_i, C_m,C_o are exaracted by the library function and a new evaluation of the TIA begins. Figure 9 shows the efficiency of this approach in progressively decreasing the total verification error during TIA optimization.
- optical receiver performance verification and correction is achieved by the simulation of the complete netlist representing the HDL-A photodiode model and the TIA structure with Eldo simulator [8]. The physical transistor dimensions representing the fast inverter are extracted directly before the optimization of the TIA has finished. For the photodiode, we extracted the final value of performance.

3. Results

As an example of the type of validation of the described approach, the method was used to design a 0.13μm CMOS $1THz\Omega$ TIA with an InGaAs PIN photodiode. With 0.01%

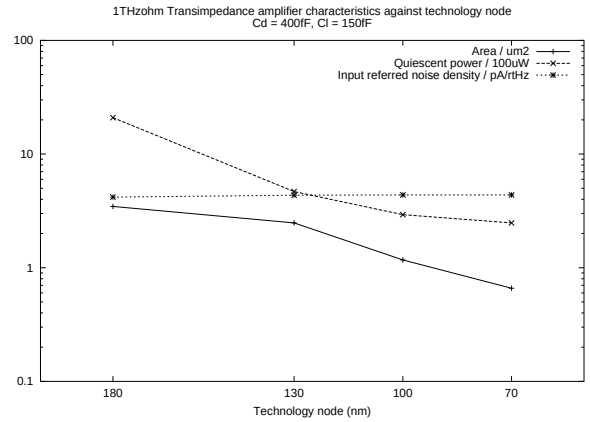


Figure 10. Transimpedance characteristics vs technology node.

precision this methodology allows a gain of more than 5x in terms of the design time requiered for manual design. The simulated photoreceiver performance is summarized in table 1.

Using this methodology and predictive BSIM3v3 models for technology nodes from 180nm down to 70nm [2], we also generated design parameters for 1THzΩ TIAs to evaluate the evolution in critical characteristics with technology node. Figure 10 shows the results of transistor level simulation of fully generated TIA circuits at each technology node. According to traditional *"shrink"* predictions, which

Table 1. Simulated performance of photoreceiver.

Parameter	Value
Optical power P_{opt}	*50* μW
Wavelength λ	*850nm*
Bandwidth BW	*1.1 GHz*
Junction capacitance C_j	*94.1 fF*
Photocurrent I_{ph}	*42.3* μA
Photodiode reverse bias voltage V_d	*1.87 V*
Intrinsic zone thickness d	*10* μm
Photodiode responsivity R	*0.85 A/W*
Transimpedance gain Z_{g0}	*62.6 db*
M_1 *transistor width* W_1	*90.4* μm
M_2 *transistor width* W_2	*4.2* μm
M_3 *transistor width* W_3	*27.0* μm
M_{1-3} *transistor lengths L*	*0.13* μm
Transimpedance feedback resistance R_f	*1.5* $k\,\Omega$
Supply voltage V_{dd}	*1.2V*
Load capacitance C_l	*6.47fF*
DC input voltage V_{in}	*0.7 V*
DC output voltage V_{out}	*0.6 V*
Quiescent power	*4.2 mW*

consider the effect of applying a unitless scale factor of $1/k$ to the geometry of MOS transistors, the quiescent power and device area should decrease with $1/k^2$ factor. Between 180nm and 70nm technology nodes $k^2 \simeq 6.61$, which is verified through our sizing optimization procedure. And finally with this methodology we can find a particular specification to a given tolerance, as shown in figure 11. With a predictive BSIM3v3 models for technology 70 nm, we have plotted the active area of the generated TIA with static power dissipation for bandwidths 1GHz to 5GHz with Zg at 1kΩ and the quality factor Q at $1/\sqrt{2}$.

4. Conclusion

The aim of the paper is to presented the implementation of a complete hierarchical synthesis methodology for

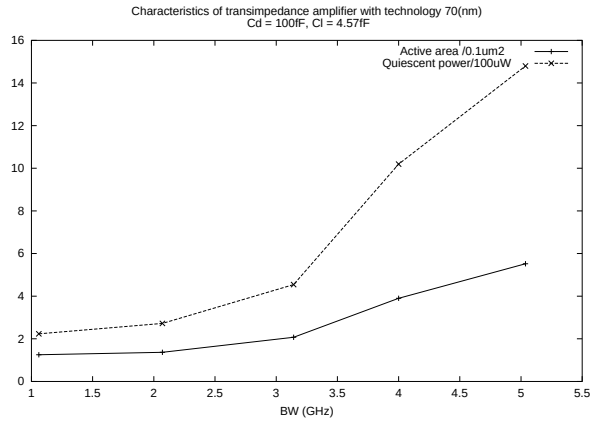


Figure 11. Transimpedance characteristics vs bandwidth node with technology 70nm.

high-speed photoreceiver front-ends. We have developed a method of communicating between different hierarchical levels based on such models. With it we can size heterogeneous systems and generate complete dimension sets for precise specifications in short synthesis times. The accurate results of this methodology have been used in the context of comparing power requirements for integrated electrical and optical links.

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