PREDICTIVE DESIGN SPACE EXPLORATION OF MAXIMUM BANDWIDTH CMOS PHOTORECEIVER PREAMPLIFIERS

Ian O'Connor, Fabien Mieyeville, Faress Tissafi-Drissi, Grzegorz Tosik and Frédéric Gaffiot

LEOM – UMR CNRS 5512
Ecole Centrale de Lyon, 36 avenue Guy de Collongue, F-69134 Ecully Cedex, FRANCE
http://leom.ec-lyon.fr/index.html

E-mail : ian.oconnor@ec-lyon.fr

ABSTRACT

This paper presents a fast and robust design method for systematically maximising the frequency response of basic CMOS transimpedance amplifiers, a class of circuit of fundamental interest to architects of MOEMS/NOEMS[1]. This method is based on a frequential analysis of the structure and a mapping of the component values to coefficients in a filter approximation function of Butterworth type. We use the method to explore the design space and examine how parametric, structural and architectural trade-offs can alleviate stringent design constraints on the internal amplifer.

1. INTRODUCTION

High-speed CMOS optical interface circuits are of profound interest to systems using optical chip-to-chip and on-chip interconnect, as they combine mainstream IC technology compatibility with data-rate/power ratios unattainable with traditional metallic interconnect [1]. The receiver (transimpedance) preamplifier is one of the most critical components in the link, since it has to cope with the large photoreceiver capacitance C_d situated at its input.

In silicon technologies, C_d can attain values as high as 500fF, which is a direct result of requiring a large area of silicon to generate a detectable current (some 10μA). One alternative is to use III-V technology photodetectors, which have a much higher sensitivity and can thus generate similar levels of current with a greatly reduced area and therefore capacitance values as low as 10fF. However, the advantage gained is offset by parasitic capacitances introduced by packaging: bond pads in typical CMOS technology have capacitances of the order of 1pF. Recourse to advanced packaging technology (MCM, flip-chip, heterogeneous integration[2]) is required to solve these issues.

In general then, the overall bandwidth of an optical link is limited by that of the transimpedance amplifier. In order for optical interconnects to be viable, and compete with (and surpass) metallic interconnect performance, bandwidths well above 1GHz are a necessity. *Ad hoc* methods exist to attain bandwidth maximization, which we categorize into three (not necessarily exclusive) groups:

- parametric: for a given transimpedance structure, find the combination of component parameters necessary for maximum bandwidth
- structural: for a given preamplifier architecture, make structural modifications, usually by adding elements such as inductors for shunt peaking [3] or capacitors as artificial loads or feedback [4]
- architectural: use more complex architectures such as bootstrap or common-gate input stages [5]

For many of these approaches, the common factor that allows bandwidth maximization is the well-known Butterworth filter response. The systems to be examined are of second or third order (for which the general equations are represented in (1) and (2) respectively):

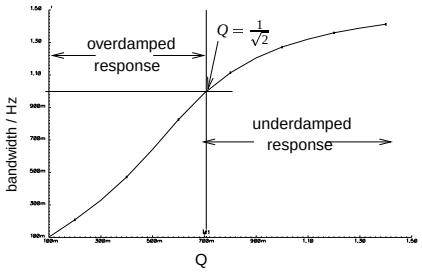
$$H(s) = \frac{A_0}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{1}$$

$$H(s) = \frac{A_0}{1 + \frac{s}{\omega_0 Q^2} + \frac{s^2}{\omega_0^2 Q^2} + \frac{s^3}{\omega_0^3}} \tag{2}$$

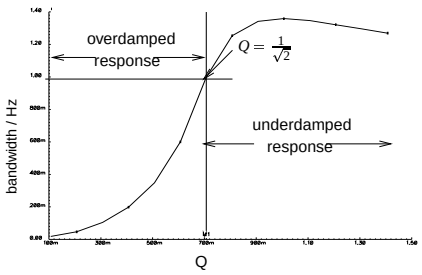
where A_0 is the low-frequency gain, ω_0 is the pole angular frequency (rad/s) and Q is the pole quality factor ($= 1/2\zeta$, where ζ is the damping factor.) The limit between over- and under-damped frequency responses (which corresponds to a flat and maximised bandwidth) occurs when $Q = 1/\sqrt{2}$, as shown in figure 1 for second and third order systems.

This paper is organized into three parts. We begin with a theoretical analysis of the basic transimpedance amplifier and develop a formulation for analytical expressions for the transimpedance gain, bandwidth and quality coefficient. By rearrangement of the analytical equations, we subsequently develop a design procedure. We end by an exploration of the design space of this structure.

[1] Micro/Nano-Opto-Electro-Mechanical Systems

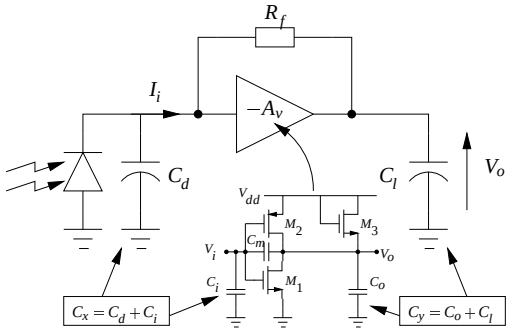


(a) Normalized second order system

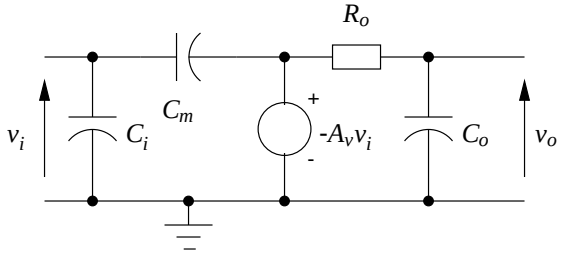


(b) Normalized third order system

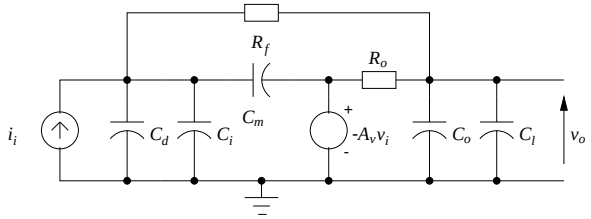
Figure 1. Bandwidth against Q



(a) Basic transimpedance amplifier



(b) Amplifier model



(c) Transimpedance amplifier circuit model

Figure 2. Models for analysis of the basic transimpedance amplifier

2. THEORETICAL ANALYSIS OF BASIC TRANSIMPEDANCE AMPLIFIER

The basic transimpedance amplifier structure in a typical configuration is shown in fig. 2(a) [6]. In this work, we target CMOS technology such that we can replace the amplifier block by a model with capacitive input impedance. The complete circuit model that we use for this first analysis is shown in fig. 2(c) (note that we model the photodiode simply as a current source with parasitic capacitance).

The expression for the transimpedance gain Z_g is then:

$$Z_g(s) = \frac{v_o}{i_i} = \frac{Z_{g0} + a_1 s}{1 + b_1 s + b_2 s^2} \tag{3}$$

where:

$$\begin{aligned} Z_{g0} &= \frac{R_o - R_f A_v}{1 + A_v} \\ a_1 &= \frac{C_m R_o}{1 + A_v} \\ b_1 &= \frac{C_x(R_o + R_f) + C_y R_o + C_m R_f (1 + A_v)}{1 + A_v} \\ b_2 &= \frac{R_o R_f (C_x C_y + C_x C_m + C_y C_m)}{1 + A_v} \end{aligned}$$

In these expressions, $C_x = C_d + C_i$ and $C_y = C_l + C_o$.

For the purposes of the approach developed in this paper, we have neglected any internal amplifier poles, which is a valid assumption as long as the amplifier structure has only one stage.

The system described in (3) is of second order, for which the general equation was given in (1). By identification,

$$Z_{g0} = \frac{R_o - R_f A_v}{1 + A_v} \tag{4}$$

$$\begin{aligned} \omega_0 &= \sqrt{\frac{1 + A_v}{R_o R_f (C_x C_y + C_m (C_x + C_y))}} \\ &= \frac{1}{R_o C_y} \sqrt{\frac{1 + A_v}{M_f (M_x + M_m + M_x M_m)}} \end{aligned} \tag{5}$$

$$\begin{aligned} Q &= \frac{\sqrt{(1 + A_v)(R_f R_o (C_x C_y + C_m (C_x + C_y)))}}{C_x (R_o + R_f) + C_y R_o + C_m R_f (1 + A_v)} \\ &= \frac{\sqrt{M_f (M_x + M_m (1 + M_x))(1 + A_v)}}{1 + M_x (1 + M_f) + M_m M_f (1 + A_v)} \end{aligned} \tag{6}$$

where we introduce the multiplying factors $M_f = R_f/R_o$, $M_i = C_x/C_y$ and $M_m = C_m/C_y$, normalizing all expressions to the time constant $\tau = R_o C_y$.

Note that in these expressions we have neglected the effect of the zero caused by the Miller capacitance C_m, supposing that its position is at a higher frequency than those of the poles, and that it therefore does not affect the bandwidth calculation. This assumption is true as long as

$$A_v > \frac{M_m^2}{M_f(M_x + M_m + M_x M_m)} - 1$$

which is likely to be valid if the Miller capacitance is merely the parasitic gate-drain capacitance in the internal amplifier. The zero could however be used to extend the bandwidth by placing it at the same position as the poles by setting:

$$M_m \gg \frac{1}{2}(M_f(1+M_x) \pm \sqrt{(M_f(1+M_x))^2 + 4M_f M_x})$$

and solving for A_v. This invariably requires an additional capacitive element in parallel with the feedback resistance, and we will not develop this approach further in this paper.

3. DESIGN PROCEDURE

Given the above analysis, we develop a design procedure which, from desired transimpedance performance criteria (Z_{g0}, bandwidth and Q) and operating conditions (C_d, C_l) generates component values for the feedback resistance R_f and the voltage amplifer (A_v and R_o). We assume initially that the amplifier has no parasitic capacitances C_i, C_m or C_o and thus does not contribute to C_x or C_y. In a hierarchical design (automation) environment, this hypothesis is revised once a transistor-level circuit has been generated from the specifications for the amplifier, as shown in fig. 3.

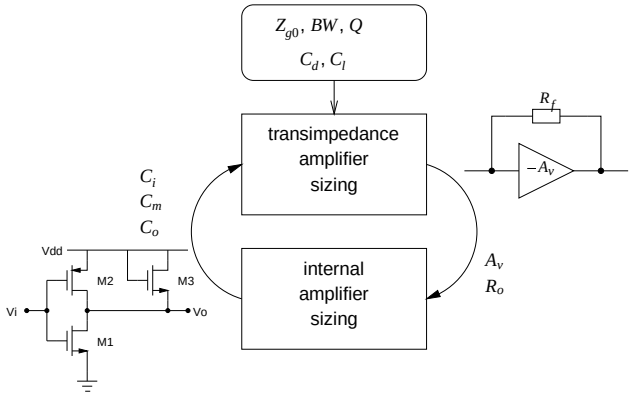


Figure 3. Hierarchical design procedure

Closed-form expressions exist for A_v, R_o and R_f but these are complex, which makes their implementation difficult and error-prone. The design procedure that we developed is iterative and works on the simple bisection principle, including a boundary detection and extension mechanism. The algorithm was implemented in Java and converges systematically in under a second (typically a few tens of iterations) to a precision of better than 0.01% on a Sun Sparc5 workstation.

Vary M_f by bisection and calculate	
$A_v = \frac{a-2bcQ^2 \pm \sqrt{a^2-4abcQ^2}}{2c^2Q^2} - 1$	if $M_m \neq 0$
$A_v = \frac{b^2Q^2}{M_f M_x} - 1$	if $M_m = 0$
$R_o = \frac{\sqrt{\frac{1+A_v}{M_x M_f}}}{\omega_0 C_y}$	
$R_f = M_f R_o$	
$Z'_{g0} = \frac{R_o - R_f A_v}{1+A_v}$	
where: $a = M_f(M_x + M_m + M_x M_m)$	
$b = 1 + M_x(1+M_f)$	
$c = M_m M_f$	
until $\lvert Z_{g0} - Z'_{g0} \rvert < \varepsilon$	

(a) Transimpedance sizing procedure

$V_{gst1} = V_i - V_{t1}$,	$V_{gst2} = V_i - V_{dd} - V_{t2}$
$g_{m1} = \frac{A_v/R_o}{\frac{V_{gst1}}{\lvert V_{gst2} \rvert}+1}$,	$\left(\frac{W}{L}\right)_1 = \frac{g_{m1}}{K_n V_{gst1}}$
$g_{m2} = g_{m1}\frac{V_{gst1}}{\lvert V_{gst2} \rvert}$,	$\left(\frac{W}{L}\right)_2 = \frac{g_{m2}}{K_p \lvert V_{gst2} \rvert}$
$L_{1,2,3} = L_{min}$,	$\left(\frac{W}{L}\right)_3 = \frac{W_{min}}{L_{min}}$

(b) First-cut sizing procedure for fast inverter

Figure 4. Algorithms for transimpedance sizing

The synthesis equations and the procedure used to calculate A_v, R_o and R_f are given in fig. 4(a), being rearrangements of the analytical equations (4), (5), (6).

4. DESIGN SPACE EXPLORATION

Taking into consideration the physical realization of the amplifier, those with requirements for low gain and high output resistance (high R_o/A_v ratio) are the easiest to build, and also require the least quiescent current and area. We have plotted this quantity against the transimpedance amplifier specifications (bandwidth and transimpedance gain) for $C_x = C_d = 500fF$ and $C_y = C_l = 100fF$ (fig. 5).

Using approximate equations for the small-signal characteristics and bias conditions of the circuit, we developed a procedure to make a first-cut sizing of the amplifier, as shown in fig. 4(b). The solution was then fine-tuned with a direct search optimization algorithm, using simulation for exact results. The parasitic device capacitances were extracted and re-injected into the transimpedance amplifier method, and the overall loop converged in fewer than five iterations (less than a minute on a Sun Ultra 5 workstation).

Using this methodology and predictive BSIM3v3 models for technology nodes from 180nm down to 70nm [7],

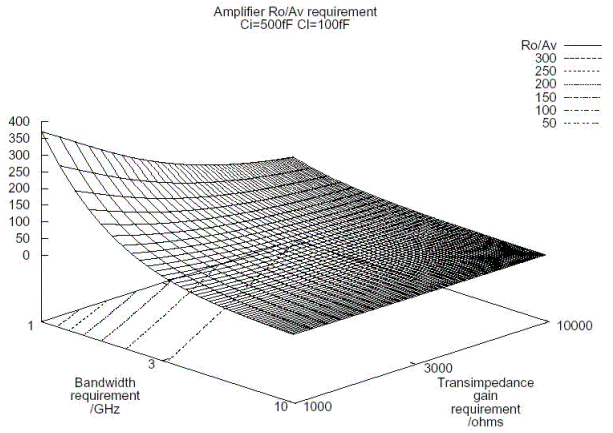
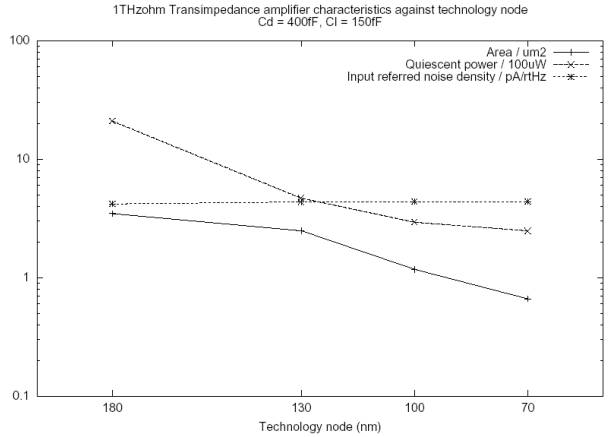
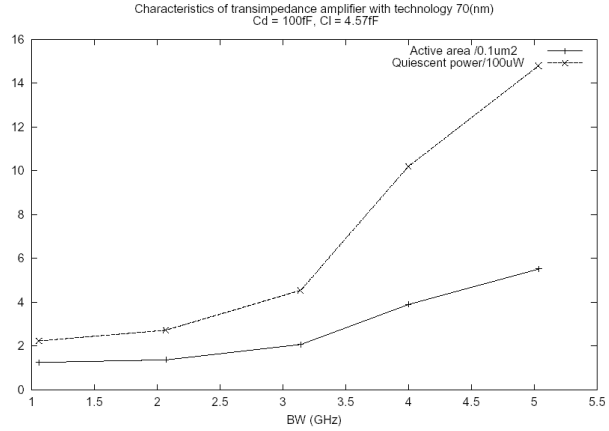


Figure 5. Design space for R_o/A_v requirements

we generated design parameters for 1THzΩ transimpedance amplifiers to evaluate the evolution in critical characteristics with technology node. Fig. 6(a) shows the results of transistor level simulation of fully generated photoreceiver circuits at each technology node. According to traditional "shrink" predictions, which consider the effect of applying a unitless scale factor of $1/k$ to the geometry of MOS transistors, the quiescent power and device area should decrease by a factor of $1/k^2$. Between the 180nm and 70nm technology nodes, $k^2 \simeq 6.61$, which is verified through our sizing optimization procedure. And finally with this methodology we can find a particular specification to a given tolerance, as shown in fig.6(b). We have plotted the active area of the generated TIA with static power dissipation for bandwidths 1GHz to 5GHz with Zg at 1kΩ and the quality factor Q at $1/\sqrt{2}$.



(a) Transimpedance characteristics vs technology node



(b) Transimpedance characteristics vs bandwidth performance for 70nm technology

Figure 6. Transimpedance characteristics vs technology node and bandwidth requirement

5. SUMMARY AND CONCLUSIONS

We have presented a design method for systematic bandwidth maximisation of basic CMOS optical receiver preamplifiers, used in high-speed optoelectronic receiver circuits. This method is easy to implement, exhibits fast execution and allows a near-exhaustive exploration of the design space in very little time. We have used this method to predict the evolution in preamplifier performance with technology.

6. REFERENCES

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