Ian O'Connor

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Born 29/8/1969, Cambridge (UK)
British national
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Professional experience

Head of Heterogeneous Systems Design Group, Vice-Director Lyon Institute of Nanotechnology JRU 5270	2007-present
Full Professor, Electronic Electrical and Control Engineering Department Ecole Centrale de Lyon, Ecully (F)	
Also Adjunct Professor, Computer Engineering Department *Ecole Polytechnique de Montréal (CA)*	*since 2008*
Associate Professor, Electronic Electrical and Control Engineering Department Ecole Centrale de Lyon, Ecully (F)	1998-2007
Senior CAD Engineer, Design Technology Centre Philips (now NXP) Semiconductors, Southampton (GB)	1997-1998
Research and teaching assistant, Microelectronics Department Institut Supérieur d'Electronique du Nord (ISEN), Lille (F)	1993-1997
Network engineer CIMM-SDI, Villeneuve d'Ascq (F)	1993

Education

Professoral Dissertation (Habilitation à Diriger des Recherches) in Electronics *"Physically heterogeneous systems on chip:* *design methodologies and optical interconnect systems"* Ecole Centrale de Lyon, Ecully (F)	Oct. 2005
PhD (with distinction) in Electronics *"Automated design of current memory cells"* Director: J.-N. Decarpigny ; Advisor: A. Kaiser University of Lille I (F)	Nov. 1997
MSc Electrical Engineering (European Program) University of Essex, Colchester (UK) / ESIEE, Paris (F) / University of Karlsruhe (D)	Jul. 1992
BEng 2/i Electronic Systems Engineering University of Essex, Colchester (UK)	Jul. 1990

Teaching activities at Ecole Centrale de Lyon

Principles of electronics	C, S
Advanced system electronics (M)	L, C, S
Introduction to autonomous microsystems (M)	L, C
Design choice management in Electrical Engineering (M)	L
System on chip design methodology	L
DSP and telecom systems (M)	L, S
Analog and mixed-signal integrated circuit design (M)	L, C, S
VLSI system architectures	S
Microsystems, microsensors, microfluidics	L, C
Micronanoelectronic circuit design (M)	L, C, S

M=course manager

L=lectures C=problem classes S=laboratory sessions

Administrative responsibilities

Vice-Director of Lyon Institute of Nanotechnology (ECL site manager)	2006-2010
Elected member of ECL Scientific Council	2001-2005
Elected member of ECL Electrical and Information Sciences Board	2001-2007
Member of ECL International Relations Board	1999-present
Chairman of ECL examination board for 2010 graduation track	2007-2009

Current research activities at Lyon Institute of Nanotechnology (INL)

Design methods for heterogeneous Systems on Chip and Systems in Package

Principal collaborations: CEA-LETI (France), STMicroelectronics (France), Ecole Polytechnique de Montréal (Canada)

This work focuses on multi-level synthesis and modeling for integrated multi-physics systems, with the two-fold objective of enabling the exploration of the impact of physical parameters on system performance, and of system constraints on component specifications. In this context, I am leading research into the establishment of a framework for multi-domain and multi-abstraction level synthesis called RuneII (Rhône-Alpes PRTP Osmose, Centre Jacques Cartier and CNRS International Scientific Cooperation projects, Nano2008 and Nano2012 agreements, French ANR^{PNANO} 3D-IDEAS).

Predictive evaluation of on-chip optical interconnect networks

Principal collaborations: CEA-LETI (France), IMEC (Belgium), STMicroelectronics (Italy), Ecole Polytechnique de Montréal (Canada)

Based on tools developed in the "Design methods for heterogeneous SoC and SiP" projects, we have explored the world's first simulation-based quantitative comparisons of electrical to optical interconnects at the physical link level (French RMNT project Heteropt, EU FP6-IST PICMOS, EU FP7-IP HELIOS). We are currently working on concurrent physical and system-level evaluations for optical networks on chip, enabling high bandwidth and low contention routing of data using wavelength multiplexing (French ACI Lambdaconnect, EU FP7-ICT WADIMOS).

Reconfigurable computing based on advanced and emerging devices

Principal collaborations: CEA-LETI (France), IMS (France)

Recent technological breakthroughs have led to the advent of advanced and emerging multiple gate devices. Such devices, with four accessible terminals, open the way to solutions specifically exploiting the additional terminal for reconfigurability purposes. We are currently leading development of digital n-function dynamically reconfigurable cells based on double-gate CNTFETs (French ACI Nanosys, ANR^{ARPEGE} Nanograin) and on double-gate MOSFETs (French ANR^{PNANO} Multigrilles).

Publications summary

- 14 articles published in refereed publications (journals)
- 9 book chapters, 2 edited books
- 17 invited/keynote and 51 regular articles published in refereed international conference proceedings
- 30 workshop presentations, seminar lectures and tutorials
- 1 patent

Principal scientific responsibilities

- Head of "Heterogeneous System Design" group at INL
- Advisor for 11 student projects, 15 MSc internships, 13 PhDs, 9 postdoctoral fellowships
- Workpackage leader for 2 regional projects, 5 national projects, 2 European projects
- Scientific coordinator for 1 regional project, 1 national project, 3 international projects
- Served as General Chair of 1 international conference (TAISA 2007), Program chair of 1 international conference (IEEE ISVLSI), Technical program committee member of 7 international conferences (DATE 2006/2010, NEWCAS-TAISA 2006-present, ReCoSoC 2006-present, ENICS 2008-present, ISVLSI 2008-present, ISIE 2007-present, DDECS 2009), Co-founder and Program Chair of 1 Winter School (FETCH 2007-present)
- Reviewer of several national (ANR) and international (ISF, SNSF) projects
- Member of French SoC-SiP Research Network steering committee: Heterogeneous Systems Chair
- Expert with AERES (French agency for the evaluation of research and higher education)
- Visiting Professor at Ecole Polytechnique de Montréal, Canada in December 2005, January 2008. Adjunct Professor at same institution since November 2008.
- IEEE Senior Member, member of IET, ACM/SIGDA, Club EEA
- Reviewer for IEEE J. Solid-State Circuits, IEEE Trans. Computer Aided Design, IEEE Trans. Electron Devices, Analog Integrated Circuits and Signal Processing, VLSI, Microelectronics Journal, Design and Test of Computers, numerous international conferences
- Expert with Nanodevices Group of the French Observatory of Micro-Nanotechnologies (OMNT) since 2005
- Reviewer for 16 PhD theses since 2005
- Board member for 4 professoral dissertations since 2007

Detailed description of research work

In the context of strong diversification and complexification of semiconductor technologies, which offer unprecedented levels of system functionality, the main objectives of my research concern the novel or more efficient uses of advanced, emerging or alternative devices in innovative System-on-Chip (SoC) and System-in-Package (SiP) architectures.

Design methods for heterogeneous Systems on Chip and Systems in Package

From the miniaturization of existing systems (position sensors, labs on chip ...) to the creation of specific integrated functions (memory, RF tuning, energy ...), MEMS and non-electronic devices are being integrated to create heterogeneous systems in package (SiP) and systems on chip (SoC). This approach for future systems, classically termed as "More than Moore", will have significant impact on several economic sectors and is driven by

- the need for the miniaturization of existing systems to benefit from technological advances and improve performance at lower overall cost,
- the potential replacement of specific functions in SoC/SiP with non-electronic devices (optical interconnect, magnetic memory, ...),
- the advent of high-performance user interfaces (virtual surgical operations, games consoles, ...),
- the rise of low-power mobile systems (communications and mobile computing) and wireless sensor networks for the measurement of phenomena inaccessible to single-sensor systems.

While the general benefits appear to be clear, this evolution represents a strong paradigm shift for the semiconductor industry, as obstacles to transistor scaling (both fundamental and economic) also push the focus towards increasing diversification. This shift away from a trend that has lasted over 40 years is possible because the fabrication technology (or at least the individual technological steps) exists to do so; however, the capacity to translate system drivers into technology requirements (and consequently guidance for investment) to exploit such diversification is severely lacking. Such a role can only be fulfilled by a radical shift in design technology to address the new and vast problem of heterogeneous system design while remaining compatible with standard "More Moore" flows.

The main objective of such an evolution is to reduce the design time in order to meet time to volume constraints. It is widely recognized that for complex systems at advanced technology nodes, a radical evolution in design tools and methods is required to reduce the "design productivity gap". Production capacity increases annually by around 50%, while design capacity increases annually by a rate of only 20-25%. All ITRS Roadmaps (and intermediate updates) since 2003 clearly state that "*Cost [of design] is the greatest threat to continuation of the semi-conductor roadmap. ... Today, many design technology gaps are crises*". Without the introduction of new design technology, design cost becomes prohibitive and leads to weak integration of high added value devices (such as sensors and RF circuits) for the various application sectors (automotive/transport, biomedical, telecommunications ...).

In this context, we are working on an experimental framework for multi-domain and multi-abstraction level synthesis called Rune[II] (scientific coordination of PRTP Osmose, Centre Jacques Cartier and CNRS International Scientific Cooperation projects, Nano2008 / Nano2012 agreements). In particular, we have worked on methods for the formalization of design processes over multiple abstraction levels and multiple domains, using a common model for design knowledge formulation called AMS IP. To address the need to represent this knowledge at higher abstraction levels in order to retain compatibility with system-level design methods, we have demonstrated the feasibility of the use of UML and established parallels between the UML concepts and widely used concepts in AMS descriptions. We are currently working on interval optimization methods exploiting response surface models based on data taken from optimally defined Design of Experiments sets of simulations, in order to take process and environmental variability into account during robust design processes. Work is also starting on analog / digital / 3D partitioning methods to enable the exploration of the full potential of architectures using 3D integration techniques (coordination of ANR[PNANO] 3D-IDEAS, participation in Eureka[CATRENE] 3DIM3).

Collaborations: CEA-LETI (France), STMicroelectronics (France), InESS (France), IMEP-LAHC (France), Ecole Polytechnique de Montréal (Canada), R3Logic (USA).

Predictive evaluation of on-chip optical interconnect

The emergence of very high performance SoC is necessary to achieve future required application performance in terms of resolution (audio, video and computing) and CPU power / total MIPS (real-time encoding-decoding, data encryption-decryption). The shift to distributed multi-processor architectures is the

recognized route to such performance and therefore requires organized high-speed communication between processors. Metallic interconnect will be highly inefficient in this role due to unachievable tradeoffs between design parameters (the main limitations due to metallic interconnects are inter-line crosstalk, latency, global throughput, connectivity and power consumption).
The concept of integrated optical interconnect is a potential technological solution to alleviate some of these issues involved in exchanging data between cores in SoC architectures. Our work aims to contribute to the ongoing assessment of the suitability of integrated optical interconnect for on-chip data transport.

Based on tools developed in the "Design methods for heterogeneous SoC and SiP" research work, we have successfully built class diagrams for functional and structural models of integrated optical link component libraries, and implemented synthesis scenarios to explore, in a detailed way, the available design space over a number of very different dimension types. This design method and technology is particularly useful for the repetitive design of fixed optical link structures subject to varying design constraints, technology parameters, and performance requirements. We have illustrated the direct application of our approach for optical link synthesis and technology performance characterization by analyzing optical link performance for several sets of photonic component parameters and CMOS technology generations. Importantly for technological development, the results of such analyses can generate useful feedback from system designers to component designers. We have thus explored simulation-based quantitative comparisons of electrical to optical interconnects at the physical link level (RMNT Heteropt, FP6-IST PICMOS, FP7-ICT HELIOS) and contributed to the development of the world's first demonstration of a working optical link on a CMOS wafer. We are currently working on concurrent physical and system-level evaluations for optical networks on chip, enabling high bandwidth and low contention routing of data using wavelength multiplexing (ACI Lambdaconnect, FP7-ICT WADIMOS), and exploring the impact of a photonic communication layer in a 3D manycore SoC.

Collaborations: CEA-LETI (France), IMEC (Belgium), STMicroelectronics (Italy), Ecole Polytechnique de Montréal (Canada).

Reconfigurable computing based on advanced and emerging devices

It is today widely recognized that transistor scaling, as a vector for the pursuit of performance and computing capacity predicted by Moore's Law and required by future software applications, will not last through the next decade. Alternatives must be found, be they at the architectural level (e.g. evolving from SoC towards MPSoC then towards reconfigurable platforms as principle computing fabric) or at the device level (heterogeneous or nanoelectronic devices). This vision, as stated by the European technological platform ARTEMIS, represents the structuring, necessary for future systems design, of several tens of billions of elementary, unreliable, nanometric devices. These systems will be used in the majority of economic sectors and in particular for high-performance computing (analysis and modeling of complex phenomena, advanced human-machine interaction) and for low-power mobile systems (sensor networks, ...)

The reconfigurable approach to computing systems comprises several advantages. It allows volume manufacturing and thus constitutes a solution to the projected evolution of mask costs (above $10M in 2011; above $100M in 2018 according to the ITRS). Such systems can cover a broad range of applications, and their performance levels very clearly exceed those of programmable systems in terms of computing speed, while requiring only one set of masks. Moreover, the natural association of these architectures with fault-tolerant design techniques makes it possible to build robust architectures in the context of increasingly unreliable elementary nanometric CMOS devices. Nevertheless, the various types of reconfigurable circuits (FPGA, coarse-grain reconfigurable systems) are at a disadvantage (compared to "full-custom" solutions) in terms of performance and device count necessary to fulfill a specific function.

In this context, the emergence of new research devices offers the opportunity to provide novel building blocks, to elaborate non-conventional techniques for reconfigurable design and consequently to reconsider the paradigms of computing architectures to achieve orders of magnitude improvements in the conventional figure of merit (MIPS / volume*power). The concept of ultra-fine grain reconfigurability enables benefits in terms of silicon real estate, since it makes it possible to reduce the number of logic cells necessary to implement a given switching function (in comparison with the implementation of these functions with conventional CMOS logic). Moreover, it makes it possible to reduce the interconnect network, which also reduces area and also the parasitic capacitances due to routing (of the interconnect network). It thus significantly reduces dynamic power dissipation and improves speed. These two performance metrics are often the weak point of programmable circuits in comparison with "full-custom" circuits because they are worsened by the parasitic capacitances of the interconnect network.

Recent technological breakthroughs have led to the advent of advanced multiple gate devices in both planar (DG MOSFET) and vertical dispositions (FinFET), as well as, more prospectively, emerging devices such as carbon nanotube transistors (CNTFET) or nanowire transistors (NWFET). Such devices, with four accessible terminals, open the way to solutions specifically exploiting the additional terminal for reconfigurability purposes.

We are currently developing reconfigurable cells based on double-gate CNTFETs (French ACI Nanosys, French ANR^{ARPEGE} Nanograin) and on double-gate MOSFETs (French ANR^{PNANO} Multigrilles). For double-gate CNTFET, we focus primarily on the specific ambivalence property, which enables p-type or n-type device behavior within the same CNTFET depending on the voltage applied to the back-gate. A family of dynamically reconfigurable multiple-function logic gates using this device and this specific property was subsequently introduced with most notably a 7-transistor dynamically reconfigurable cell with 14 accessible boolean functions. From first layout and simulations we have estimated elementary performance metrics and compared them to conventional CMOS techniques, demonstrating significant power savings for comparable speeds. For DGMOS devices in DG FD SOI/CMOS technology, particularly those with asymmetric oxide thicknesses for the front and back gates and independently controlled gates, a similar type of family of cells has been devised, demonstrating significant gate area reductions compared to conventional CMOS LUT techniques, while configuration memory requirements are also reduced. A 2-input reconfigurable cell used as a benchmark was implemented in both static and dynamic logic styles. It can be used either as an all-asymmetric device variant with low V_{dd} in low power reconfigurable applications or as a mixed-device variant with a higher V_{dd} to achieve comparable speeds to CMOS-LUTs. These types of cell can be used in fixed interconnect matrices connected by switchboxes, and we have also developed a method to map function graphs representing complex logical functions to such matrices. We have applied the exhaustive use of these methods to identify the success rate of mapping functions to matrices, and are currently working on partitioning increasingly complex functions across matrices, and on building a complete cluster-based architecture based on such matrices.

Collaborations: CEA-LETI (France), IMS (France), Ecole Polytechnique de Montréal (Canada)

List of publications for Ian O'Connor

Edited books

1. *Heterogeneous Embedded Systems: Design Theory and Practice*, ed. I. O'Connor, G. Nicolescu, C. Piguet, Springer, *in preparation (2010)*
2. *Integrated Optical Interconnect Architectures and Applications in Embedded Systems*, ed. I. O'Connor, G. Nicolescu, Springer, *in preparation (2011)*

Book chapters

1. F. Mieyeville, M. Brière, I. O'Connor, F. Gaffiot, G. Jacquemod, "A VHDL-AMS library of hierarchical optoelectronic device models, " in *Languages for System Specification and Verification*, ed. C. Grimm, pp. 145-161, Kluwer, 2004
2. I. O'Connor, F. Gaffiot, "Advanced research in on-chip optical interconnects," in *Low power electronics design*, ed. C. Piguet, CRC press, 2004
3. I. O'Connor, F. Gaffiot, "On-chip optical interconnect for low-power," in *Ultra-low power electronics and design*, ed. E. Macii, Kluwer Academic Publishers, 2004
4. I. O'Connor, F. Tissafi-Drissi, G. Revy, and F. Gaffiot, "UML/XML-based approach to hierarchical AMS synthesis," in *Advances in Specification and Design Languages for SoCs*, ed. A. Vachoux, Kluwer Academic Publishers, 2006
5. J. Gautier, I. O'Connor, "Intégration tridimensionnelle," in *Synthèse de l'année 2007 – Nanocomposants : Les avancées de l'année 2007*, pp. 35-36, ed. S. Fontanell, Observatoire des Micro et NanoTechnologies, 2008
6. I. O'Connor, I. Hassoune, X. Yang, D. Navarro, "Logic circuit design with DGMOS devices," in *Planar Double-Gate Transistor: Technology and Design*, ed. A. Amara, O. Rozeau, Springer, 2009
7. P. Freitas, D. Navarro, I. O'Connor, G. Billiot, H. Lapuyade, J.-B. Begueret, "Analog circuits design," in *Planar Double-Gate Transistor: Technology and Design*, ed. A. Amara, O. Rozeau, Springer, 2009
8. I. O'Connor, I. Hassoune, D. Navarro, "Fine-Grain Reconfigurable Logic Cells Based on Double-Gate MOSFETs," in *VLSI-SOC: Design Methodologies for SoC and SiP*, ed. D. Soudris, C. Piguet, R. Reis, Springer, 2009
9. I. O'Connor, "Platform for model-based design of integrated multi-technology systems," in *Model-Based Design for Embedded Systems*, ed. P. Mostermann, G. Nicolescu, CRC Press, 2009

Articles published in refereed publications (journals)

1. F. Gaffiot, K. Vuorinen, F. Mieyeville, I. O'Connor, G. Jacquemod, "Behavioral modeling for hierarchical simulation of optronic systems," *IEEE Transactions on Circuits and Systems - II. Analog and Digital Signal Processing*, vol. 46, no. 10, pp. 1316-1322, October 1999
2. B. Stefanelli, I. O'Connor, L. Quiquerez, A. Kaiser, D. Billet, "An analog beam-forming circuit for ultrasound imaging using switched-current delay lines," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 202-211, February 2000
3. I. O'Connor, A. Kaiser, "Automated synthesis of switched-current cells," *IEEE Transactions on Computer Aided Design*, vol. 19, no. 4, pp. 413-424, April 2000
4. P. Bontoux, I. O'Connor, F. Gaffiot, X. Letartre, G. Jacquemod, "Behavioral modeling and simulation of optical integrated devices," *Special Section of Analog Integrated Circuits and Signal Processing*, vol.29, issue 1/2, pp.37-47, october 2001
5. G. Tosik, F. Gaffiot, Z. Lisik, I. O'Connor, F. Tissafi-Drissi, "Power dissipation in optical and metallic clock distribution networks in new VLSI technologies," *Electronics Letters*, vol. 4, no. 3, pp. 198-200, 5 February 2004
6. A. Kazmierczak, M. Brière, E. Drouard, P. Bontoux, P. Rojo-Romeo, I. O'Connor, X. Letartre, F. Gaffiot, R. Orobtchouk, T. Benyattou, "Design, Simulation and Characterization of a Passive Optical Add-Drop Filter in Silicon-On-Insulator Technology," *Photonics Technology Letters*, vol. 17, no. 7, pp. 1447 – 1449, July 2005

7. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Design of a Novel CNTFET-based Reconfigurable Logic Gate," *Electronics Letters*, vol. 43, no. 9, pp. 514-516, 26 April 2007
8. I. O'Connor, F. Tissafi-Drissi, F. Gaffiot, J. Dambre, M. De Wilde, D. Stroobandt, J. Van Campenhout, D. Van Thourhout, "Systematic Simulation-Based Predictive Synthesis of Integrated Optical Interconnect," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*,vol. 15, no. 8, pp. 927-940, August 2007
9. A. Kazmierczak, E. Drouard, M. Brière, P. Rojo-Romeo, X. Letartre, I. O'Connor, F. Gaffiot, Z. Lisik, "Optimization of an integrated optical crossbar in SOI technology for optical networks on chip," *Journal of Telecommunications and Information Technology*, 3/2007, pp. 109-114, September 2007
10. I. O'Connor, J. Liu, F. Gaffiot, F. Prégaldiny, C. Lallement, C. Maneux, J. Goguet, S. Frégonèse, T. Zimmer, L. Anghel, T. Dang, R. Leveugle, "CNTFET Modeling and Reconfigurable Logic Circuit Design," *IEEE Trans. Circuits and Systems – I. Regular Papers*, vol. 54, no. 11, pp. 2365-2379, November 2007
11. I. Hassoune, I. O'Connor, "Double-Gate MOSFET Based Reconfigurable Cells," *Electronics Letters*, vol. 43, no. 23, pp. 1273-1274, 8 November 2007
12. I. Hassoune, X. Yang, I. O'Connor, D. Navarro, "Ultra-Low Power Full Adder Circuit Using SOI Double-Gate MOSFET Devices," *Electronics Letters*, vol. 44, no. 18, pp. 1095-1096, 28 August 2008
13. I. Hassoune, D. Flandre, I. O'Connor, J.D. Legat, "ULPFA: a new efficient design of a power aware full adder," *IEEE Trans. Circuits and Systems – I. Regular Papers*, accepted for publication (2009)
14. I. O'Connor, J. Liu, D. Navarro, R. Daviot, N. Abouchi, P.E. Gaillardon, F. Clermidy, "Molecular electronics and reconfigurable logic," *Int. J. Nanotechnology,* accepted for publication (2009)

Invited articles published in refereed international conference proceedings

1. I. O'Connor, "EDA Tools and Methods for Synthesis of Analog, Mixed-Signal and Mixed-Domain Integrated Systems," *Summer School of Microelectronics*, Lodz (Pologne), 25-28 septembre 2002
2. I. O'Connor, "Interconnexions optiques intégrées pour les systèmes sur puce," *Microsystèmes à cœur optique*, Marseille, 5 février 2004
3. I. O'Connor, "Invited Talk: Optical solutions for system-level interconnect," *System-Level Interconnect Prediction*, pp. 79-88, Paris, France 14-15 February 2004
4. C. Piguet, J. Gautier, C. Heer, I. O'Connor, U. Schlichtmann, "Extremely Low-Power Logic," *Design Automation and Test in Europe*, pp. 656-661, Paris, France, 16-20 February 2004
5. I. O'Connor, M. Brière, E. Drouard, A. Kazmierczak, F. Tissafi-Drissi, D. Navarro, F. Mieyeville, J. Dambre, D. Stroobandt, J.-M. Fedeli, Z. Lisik, F. Gaffiot, "Towards reconfigurable optical networks on chip," *Reconfigurable Communication centric SoCs, Montpellier*, France, 27-29 June 2005
6. F. Gaffiot, M. Brière, E. Drouard, A. Kazmierczak, D. Navarro, F. Mieyeville, G. Tosik, Z. Lisik, I. O'Connor, "Network on Chip: An Optical Alternative?" *Multiconference on Systemics, Cybernetics and Informatics*, Orlando, Florida, USA, 10-13 July 2005
7. I. O'Connor, F. Tissafi-Drissi, D. Navarro, F. Mieyeville, F. Gaffiot, J. Dambre, M. De Wilde, D. Stroobandt, M. Brière, "Integrated optical interconnect for on-chip data transport," *IEEE-NEWCAS Conference*, June 18-21, 2006, Gatineau, Canada
8. I. O'Connor, J. Liu, F. Gaffiot, "CNTFET-based logic circuit design," *IEEE Int. Conf. Design & Test of Integrated Systems in Nanoscale Technology*, Tunis, Tunisia, 5-7 Septembre 2006
9. I. O'Connor, B. Courtois, K. Chakrabarty, N. Delorme, M. Hampton, J. Hartung, "Heterogeneous Systems on Chip and Systems in Package," *Design Automation and Test in Europe*, Nice, France, 16-20 April 2007
10. I. O'Connor, H. Charlery, "Synthesis of physically heterogeneous systems on chip," *IEEE-MWSCAS/NEWCAS Conference*, August 5-8, 2007, Montreal, Canada, pp. 634-637
11. I. O'Connor, J. Liu, D. Navarro, I. Hassoune, S. Burignat, F. Gaffiot, "Ultra-Fine Grain reconfigurability Using CNTFETs," *IEEE International Conference on Electronics, Circuits and Systems*, 11-14 December 2007, Marrakech, Morocco
12. I. O'Connor, J. Liu, D. Navarro, F. Gaffiot, "Dynamically Reconfigurable Logic Gate Cells and Matrices using CNTFETs," *IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era*, 26-28 March 2008, Tozeur, Tunisia

13. F. Gaffiot, I. O'Connor, "Integrated optical interconnects: what could be possible?", Keynote, *12th IEEE Workshop on Signal Propagation on Interconnects*, 12-15 May 2008, Avignon, France
14. I. O'Connor, F. Mieyeville, F. Gaffiot, A. Scandurra, G. Nicolescu, "Can integrated photonics solve MPSoC interconnect issues?" *Int. VLSI/ULSI Multilevel Interconnection Conference,* 27-30 October 2008, Fremont (CA), USA
15. D. Van Thourhout, I. O'Connor, A. Scandurra, L. Liu, W. Bogaerts, S. Selvaraja, "Nanophotonic Devices for Optical Networks-On-Chip," *Conference on Lasers and Electro-Optics (CLEO)*, May 31 – June 5, 2009, Baltimore (MD), USA
16. I. O'Connor, "Emerging technologies and nanoscale computing fabrics," Keynote, *17th IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, October 12-14 2009, Florianopolis, Brazil
17. L. Labrak, I. O'Connor, "Heterogeneous System Design Platform and Perspectives for 3D Integration," *International Conference on Microelectronics (ICM)*, 19-22 December 2009, Marrakech, Morocco

Articles published in refereed international conference proceedings

1. I. O'Connor, A. Kaiser, "Automated design of switched-current cells," *Proc. Custom Integrated Circuits Conference*, pp. 477-480, Santa-Clara (USA), May 1998
2. B. Stefanelli, I. O'Connor, L. Quiquerez, A. Kaiser, D. Billet, "An analog beam-forming circuit using switched-current delay lines," *Proc. European Solid-State Circuits Conference*, pp. 300-303, The Hague (Netherlands), Sep. 1998
3. P. Bontoux, I. O'Connor, F. Gaffiot, G. Jacquemod, "Design and optimization of passive components for optical interconnects," *DTIP'2000*, Paris, May 9-11, 2000
4. P. Bontoux, F. Mieyeville, I. O'Connor, F. Gaffiot, G. Jacquemod, "Design and optimization of optical links based on VHDL-AMS modeling," *BMAS'2000*, Orlando, FL, USA, October 19-20, 2000, p.62-67
5. F. Mieyeville, G. Jacquemod (Esinsa), I. O'Connor, F. Gaffiot, "Behavioral modeling of short distance optical interconnects," *ISMA 2000*, Singapore, 27 November-2 December 2000, SPIE Proceedings vol. 4228, n°02, pp 1-8
6. I. O'Connor, F. Mieyeville, F. Tissafi-Drissi, F. Gaffiot, "Exploration paramétrique d'amplificateurs de transimpédance CMOS à bande passante maximisée," *Colloque sur le Traitement Analogique de l'Information, du Signal et ses Applications*, Paris, septembre 2002
7. F. Mieyeville, F. Gaffiot, I. O'Connor, J. Oudinot , P. Raynaud, F Mkalech, "VCSEL-based Optical Communication Link Simulation using VHDL-AMS," *DATE 2003*, Exhibition forum, Session X
8. M. Brière, F. Gaffiot, I. O'Connor, L. Carrel, "Integration of an FDTD algorithm in an electronic design framework," *5th International Workshop on Computational Electromagnetics*, pp. 21-26, Halifax, Canada, 17-19 June 2003
9. F. Tissafi-Drissi, I. O'Connor, F. Mieyeville, F. Gaffiot, "Design methodologies for high-speed CMOS photoreceiver front-ends," *16th Symposium On Integrated Circuits And System Design*, pp. 323-328, Sao Paolo, Brazil, 8-11 September 2003
10. G. Tosik, F. Gaffiot, Z. Lisik, I. O'Connor, F. Tissafi-Drissi, "Optical versus metallic interconnections for clock distribution networks in new VLSI technologies," *13th International Workshop on Power and Timing Modeling, Optimization and Simulation*, PATMOS 2003, pp. 461-470, Torino, Italy, 10-12 September 2003
11. G. Tosik, F. Gaffiot, Z. Lisik, I. O'Connor, "Optical versus Electrical Clock System in Future VLSI Technologies," *IEEE International SOC Conference*, pp. 261-262, Portland, USA, 17-20 September 2003
12. F. Mieyeville, M. Brière, I. O'Connor, F. Gaffiot, G. Jacquemod, "A VHDL-AMS library of hierarchical optoelectronic device models," *Forum on Specification and Design Languages*, pp. 7-18, Frankfurt, Germany, 23-26 September 2003
13. F. Tissafi-Drissi, I. O'Connor, F. Mieyeville, F. Gaffiot, "Hierarchical synthesis of high-speed CMOS photoreceiver front-ends using a multi-domain behavioral description language," *Forum on Specification and Design Languages*, pp. 151-162, Frankfurt, Germany, 23-26 September 2003
14. F. Tissafi-Drissi, I. O'Connor, F. Mieyeville, G. Tosik, F. Gaffiot, "Méthodologie de conception d'un photo-récepteur CMOS à haut-débit," *Colloque sur le Traitement Analogique de l'Information, du Signal et ses Applications*, pp. 119-122, Louvain-la-Neuve, Belgique, 25-26 septembre 2003

15. M. Brière, F. Mieyeville, I. O'Connor, F. Gaffiot, "Un réseau d'interconnexion optique passif basé sur le routage en longueur d'onde," *Symposium en Architecture et Adéquation Algorithme Architecture*, pp. 425-432, La Colle-sur-Loup, France, 15-17 octobre 2003
16. I. O'Connor, F. Mieyeville, F. Tissafi-Drissi, G. Tosik, F. Gaffiot, "Predictive Design Space Exploration of Maximum Bandwidth CMOS Photoreceiver Preamplifiers," *IEEE International Conference on Electronics, Circuits and Systems*, pp. 483-486, Sharjah, United Arab Emirates, 14-17 December 2003
17. F. Tissafi-Drissi, I. O'Connor, F. Gaffiot, "RUNE: Platform for automated design of integrated multi-domain systems. Application to high-speed CMOS photoreceiver front-ends," *Design Automation and Test in Europe*, pp. 16-21, Paris, France, 16-20 February 2004
18. G. Tosik, Z. Lisik, M. Langer, F. Gaffiot, I. O'Connor, "Simulation of Electrical and Optical Interconnections for Future VLSI ICs," *International Conference on Computational Science*, pp.1037-1044, Krakow, Poland, 6-9 June 2004
19. M. Brière, L. Carrel, T. Michalke, F. Mieyeville, I. O'Connor, F. Gaffiot, "Design and behavioural modelling tools for optical networks on chip," *Design Automation and Test in Europe*, pp. 738-739, Paris, France, 16-20 February 2004
20. E. Drouard, M. Brière, F. Mieyeville, I. O'Connor, X. Letartre and F. Gaffiot, "Optical Network On-chip Multi-Domain modeling using SystemC," *Proc. Forum on Specification and Design Languages*, pp. 123--134, Lille, France, 14-17 September 2004
21. M. Brière, E. Drouard, F. Tissafi-Drissi, F. Mieyeville, I. O'Connor and F.Gaffiot, "SystemC modeling of an Optical Network-on-Chip using VCI protocol," *Proc. GSPx*, Santa Clara, CA, USA, September 2004
22. E. Drouard, M. Brière, A. Kazmierczak, X. Letartre, I. O'Connor, F. Gaffiot, "Phenomenological modeling of WDM crossbars based on channel drop filters," *13th International Workshop on Optical Waveguide Theory and Numerical Modelling (OWTNM 2005)*, 8 – 9 April 2005, Grenoble
23. A. Kazmierczak, M. Brière, E. Drouard, P. Rojo-Romeo, I. O'Connor, X. Letartre, F. Gaffiot, L. El Melhaoui, P.Lyan, J.M. Fedeli, "Design and characterisation of optical networks on chip," *12th European Conference on Integrated optics (ECIO 2005)*, 6 – 8 April 2005, Grenoble
24. M. Brière, E. Drouard, F. Mieyeville, D. Navarro, I. O'Connor, F. Gaffiot, "Heterogeneous modelling of an optical network on chip with SystemC," *Proc. IEEE Internation Workshop on Rapid System Prototyping*, pp. 10-16, Montreal, Canada, 8-10 June 2005
25. M. Owczarek, I. O'Connor, "Program RUNE as an Example of Usage of Computers in Optimization Processes," *International Conference Microtherm*, Lodz (Poland), 19-22 June 2005
26. I. O'Connor, F. Tissafi-Drissi, G. Revy, F. Gaffiot, "UML/XML-based approach to hierarchical AMS synthesis," *Proc. Forum on Design Languages*, pp. 89-100, Lausanne, Switzerland, September 27-30 2005
27. D. Navarro, D. Ramat, F. Mieyeville, I. O'Connor, F. Gaffiot, "VHDL & VHDL-AMS modeling and simulation of a CMOS imager IP," *Proc. Forum on Design Languages*, pp. 179-182, Lausanne, Switzerland, September 27-30 2005
28. D. Navarro, M. Brière, Ian O'Connor, F. Mieyeville, F. Gaffiot, L. Carrel, "Quantitative study of area and power consumption costs for 3 Gbits/s optical communications in a 0.13µm CMOS circuit," *20th Conference on Design of Circuits and Integrated Systems*, Lisbon, Portugal, 23–25 November 2005
29. B. Payet, P. Vincent, I. O'Connor, F. Gaffiot, "A fully-integrated 60 GHz VCO in l3Onm SOI-CMOS on high-resistivity substrate," *Ph. D. Research in Microelectronics and Electronics (PRIME)*, pp. 105-108, Otranto (Lecce), Italy, 12-15 June 2006
30. S. Dia, F. Mieyeville, I. O'Connor, F. Gaffiot, "Modeling and simulation of radiofrequency circuit blocks for performance evaluation in a system-on-chip context," *Int. Symp. on Performance Evaluation of Computer and Telecommunication Systems*, Calgary, Canada, July 31-August 2, 2006
31. S. Dia, F. Mieyeville, I. O'Connor, F. Gaffiot, "Radio-frequency link modelling and simulation in a system-on-chip context," *European Modelling Symposium*, London, United Kingdom, 11-12 September 2006
32. M. Owczarek, G. Tosik, Z. Lisik, I. O'Connor, "Optimization of the On-Chip Optical Receivers," *IXth International Conference CADSM*, pp. 130-133, Polyana (Ukraine), 20-24 February 2007
33. Matthieu Brière, Bruno Girodias, Youcef Bouchebaba, Gabriela Nicolescu, Fabien Mieyeville, Frédéric Gaffiot, Ian O'Connor, "System Level Assessment of an Optical NoC in an MPSoC Platform," *Design Automation and Test in Europe (DATE)*, Nice, France, 16-20 April 2007

34. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Design of a Novel CNTFET-based Reconfigurable Logic Gate," *IEEE Symp. VLSI*, Porto Alegre, Brazil, 9-11 May 2007
35. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Novel CNTFET-based Reconfigurable Logic Gate Design," *Design Automation Conference (DAC)*, San Diego, CA, USA, 4-8 June 2007
36. M. Brière, L. Gheorghe, G. Nicolescu, I. O'Connor, "Formalisation of Optical Networks on Chip using DEVS Formalism," *Summer Computer Simulation Conference*, 14-19 Juillet 2007, San Diego, Ca, USA
37. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Design of a Family of Novel CNTFET-based Dynamically Reconfigurable Logic Gates," *IEEE-MWSCAS/NEWCAS Conference*, August 5-8, 2007, Montreal, Canada, pp. 698-701
38. I. Hassoune, I. O'Connor, D. Navarro, "On the performance of Double-Gate MOSFET circuit applications," *IEEE-MWSCAS/NEWCAS Conference*, August 5-8, 2007, Montreal, Canada, pp. 558-561
39. M. Brière, B. Girodias, Y. Bouchebaba, G. Nicolescu, F. Mieyeville, F. Gaffiot, I. O'Connor, "Architectural Exploration of Optical and Electrical Interconnects in MPSoC," *IEEE-MWSCAS/NEWCAS Conference*, August 5-8, 2007, Montreal, Canada, pp. 1469-1472
40. M. Brière, L. Gheorghe, G. Nicolescu, I. O'Connor, "Towards the High-Level Design of Optical Networks-on-Chip: Formalization of Opto-Electrical Interfaces," *IEEE International Conference on Electronics, Circuits and Systems*, 11-14 December 2007, Marrakech, Morocco
41. I. Hassoune, X. Yang, I. O'Connor, D. Navarro, "Using SOI Double-Gate MOSFET NDR Structures to Improve Ultra-Low Power Full Adder Performance," *IEEE-NEWCAS/TAISA Conference*, June 22-25, 2008, Montreal, Canada
42. I. Hassoune, I. O'Connor, D. Navarro, "Design of a Family of Gate-level Reconfigurable Logic Cells Based on Double-Gate MOSFETs," *16th IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, October 13-15 2008, Rhodes Island, Greece
43. J. Liu, I. O'Connor, D. Navarro and F. Gaffiot, "Dynamically reconfigurable CNTFET logic cell matrix programming methods," *16th IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC)*, October 13-15 2008, Rhodes Island, Greece
44. I. O'Connor, F. Mieyeville, F. Gaffiot, A. Scandurra, G. Nicolescu, "Reduction methods for adapting optical network on chip topologies to specific routing applications," *Design of Circuits and Integrated Systems (DCIS)*, November 12-14 2008, Grenoble, France
45. A. Scandurra, I. O'Connor, "Scalable CMOS-compatible photonic routing topologies for versatile networks on chip," *International Workshop on Network on Chip Architectures (NocArc)*, November 8th 2008, Lake Como, Italy
46. H. Filiol, I. O'Connor, D. Morche, "A new approach for variability analysis of analog ICs," *IEEE-NEWCAS/TAISA Conference*, June 29 – July 1, 2009, Toulouse, France
47. P.-E. Gaillardon, I. O'Connor, J. Liu, R. Daviot, N. Abouchi, F. Clermidy, "Interconnection scheme and associated mapping method of reconfigurable cell matrices based on nanoscale devices," *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, July 30-31 2009, San Francisco (CA), USA
48. H. Filiol, I. O'Connor, D. Morche, "Piecewise-Polynomial Modeling for Analog Circuit Performances", *European Conference on Circuit Theory & Design (ECCTD'09)*, 23-27 August 2009, Antalya, Turkey
49. P.-E. Gaillardon, I. O'Connor, J. Liu, R. Daviot, N. Abouchi, F. Clermidy, "Interconnection scheme and associated mapping method of reconfigurable cell matrices based on nanoscale devices," *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 13-16 December 2009, Hammamet, Tunisia
50. P.-E. Gaillardon, F. Clermidy, I. O'Connor, "Reconfigurable logic cells for nanoscale – Comparison between density and functionality enhancement," *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 13-16 December 2009, Hammamet, Tunisia
51. A. Allam, I. O'Connor, "Optical NOC Design-Parameters Exploration and Analysis," *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 13-16 December 2009, Hammamet, Tunisia

Workshop presentations

1. I. O'Connor, A. Kaiser, "Synthèse de circuits à courants commutés," *Colloque CAO de Circuits Intégrés et Systèmes*, Villard de Lans, 1997, p. 2-5

2. G. Jacquemod, I. O'Connor, F. Gaffiot, "Microelectronics education and research at Ecole Centrale de Lyon," *SAME 98*, Sophia Antipolis, October 29th 1998
3. F. Mieyeville, F. Gaffiot, I. O'Connor, G. Jacquemod, "Modélisation comportementale de liens optiques pour des interconnexions à courte distance," *Colloque CAO de Circuits Intégrés et Systèmes*, Aix en Provence, 1999, p. 209-212
4. F. Gaffiot, G. Jacquemod, P. Bontoux, F. Mieyeville, I. O'Connor, "Behavioral modeling of photonic and optronic systems," *2nd CFDRC Workshop on MEMS Simulation Technology*, Berlin, June 1999
5. F. Mieyeville, G.Jacquemod, F.Gaffiot, I. O'Connor, "Modèle thermo-opto-électronique de VCSEL pour la simulation de liens optiques pour des interconnexions à courte distance," *3émes Journées Nationales du Réseau Doctoral de Microélectronique*, Montpellier, 4-5 Mai 2000
6. F. Mieyeville, F.Gaffiot, I. O'Connor, G.Jacquemod, "Modélisation d'un lien optique inter et intra puce à haut débit," *11èmes Rencontres Régionales de la Recherche*, Saint Etienne, 20 septembre 2000
7. M. Brière, F. Gaffiot, I. O'Connor, F. Mieyeville, "Modélisation comportementale d'un détecteur de fluorescence," *7èmes Journées Pédagogiques du CNFM*, Saint Malo, novembre 2002
8. F. Tissafi-Drissi, I. O'Connor, F. Mieyeville, F. Gaffiot, "Sur l'utilisation de la logique floue dans la synthèse de circuits analogiques," *7èmes Journées Pédagogiques du CNFM*, Saint Malo, novembre 2002
9. F. Mieyeville, F. Gaffiot, I. O'Connor, J. Oudinot , P. Raynaud and F Mkalech, "VCSEL-based Optical Communication Link Simulation using VHDL-AMS," DATE 2003, Exhibition Forum, Session X
10. M. Brière, F. Mieyeville, I. O'Connor and F. Gaffiot, "Un réseau d'interconnexion optique passif basé sur le routage en longueur d'onde," Symposium en Architecture et Adéquation Algorithme Architecture, pp. 425-432, La Colle-sur-Loup, France, 15-17 octobre 2003
11. E. Drouard, M. Brière, X. Letartre, F. Mieyeville, I. O'Connor, F. Gaffiot, "Modélisation phénoménologique de réseaux WDM sur puce," Journées Nationales d'Optique Guidée, Paris, octobre 2004
12. M. Brière, T. Michalke, I. O'Connor, F. Mieyeville, D. Navarro, F. Gaffiot, "Modélisation de composants photoniques sous Matlab et VHDL-AMS pour la simulation de réseaux optiques sur puce," 8èmes Journées Pédagogiques du CNFM, Saint Malo, décembre 2004
13. M. Le Helley, F. Mieyeville, D. Navarro, I. O'Connor, "Conception d'un microprocesseur RISC," 8èmes Journées Pédagogiques du CNFM, Saint Malo, décembre 2004
14. I. O'Connor, F. Tissafi-Drissi, D. Navarro, F. Mieyeville, F. Gaffiot, J. Dambre, M. De Wilde, D. Stroobandt, D. Van Thourhout, "Optical interconnect for on-chip data communication" (invited), *DATE Workshop on Future Interconnect and Networks on Chip*, Munich, Germany, 10 March 2006
15. W. Heirman, J. Dambre, I. O'Connor, J. Van Campenhout, "Reconfigurable Optical Networks for On-Chip Multiprocessors," *DATE Workshop on Future Interconnect and Networks on Chip*, Munich, Germany, 10 March 2006
16. I. O'Connor, P. Garda, "Plate-forme STIC RFVSOC," *3ème workshop CNRS RECAP*, Lyon, 17 November 2006
17. J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, "Reconfigurable computing with emerging devices," *Keio-ECL Nanoworkshop*, Ecully, 24 November 2006
18. I. O'Connor, "Gate-level reconfigurability using asymmetric double-gate MOSFET devices," *Keio-ECL Nanoworkshop*, Yokohama, 5 November 2007
19. S. Lebeux, G. Nicolescu, I. O'Connor, "System-Level Exploration for 3D MPSoCs including Optical Networks-on-Chip," MPSoC 2009, 2-7 August 2009, Savannah (GA), USA

Seminar lectures and tutorials

1. I. O'Connor, "Le Laboratoire d'Electronique, Optoélectronique et Microsystèmes de l'Ecole Centrale de Lyon," *Escola Polytechnica de l'Université de Sao Paolo*, 12 septembre 2003
2. I. O'Connor, "Interconnexions Optiques Intégrées," *Action Spécifique "SOC et Nouvelles Technologies" (RTP SOC)*, Paris, 10 décembre 2003
3. E. Belhaire, P. Desgreys, P. Fouillat, P. Garda, Y. Hervé and I. O'Connor, "Présentation finale de l'Action spécifique SOC AMS," *Workshop RTP SOC*, La Londe les Maures, 18 mai 2004

4. E. Belhaire, N. Drach-Temam, P. Garda and I. O'Connor, "Présentation de l'Action Spécifique SOC et Nouvelles Technologies," *Workshop RTP SOC*, La Londe les Maures, 18 mai 2004
5. I. O'Connor, "Interconnexions optiques intégrées," *Séminaire LIRMM*, Montpellier, 11 février 2005
6. I. O'Connor, "Heterogeneous Systems on Chip: Design methodologies and integrated optical interconnect," *Séminaire ReSMiQ / Ecole Polytechnique de Montréal*, 5 décembre 2005
7. I. O'Connor, "Conception de cellules reconfigurables à base de composants avancés et émergents," *Séminaire L2MP*, Marseille, 6 décembre 2007
8. I. O'Connor, "Reconfigurable cells based on advanced and emerging double gate devices," *Séminaire ReSMiQ / Ecole Polytechnique de Montréal*, 18 January 2008
9. I. O'Connor, D. Van Thourhout, J.-M. Fedeli, "Process and design technology for on-chip optical interconnect," *Int. VLSI/ULSI Multilevel Interconnection Conference,* 27-30 October 2008, Fremont (CA), USA
10. I. O'Connor, "Optical interconnect for future systems on chip," *Séminaire ETIS*, Paris, 3 février 2009
11. I. O'Connor, "Logic architectures with emerging technologies," *MSc Erasmus Tutorial*, TU Lodz, 21 June 2009

Patents

1. I. O'Connor, I. Hassoune, "Cellule logique reconfigurable à base de transistors MOSFET double grille," *Brevet français* n°07 56487, 13 juillet 2007

Theses

1. I. O'Connor, "Josephson contact based digital-analog converter structures," *Diplomarbeit*, Universität Karlsruhe (D), 1992, 82 p.
2. I. O'Connor, "Automated design of switched-current cells," *Thèse de doctorat*, Université de Lille I, 1997, 224 p.
3. I. O'Connor, "Systèmes sur puce physiquement hétérogènes : Méthodologies de conception et Systèmes optiques d'interconnexion," *Habilitation à Diriger des Recherches*, Ecole Centrale de Lyon, 2005, 142 p.

Supervision and training activities[1]

MSc students

Name	*Nature of degree*	*Period*	*Funding*	*% co-supervision*	*Title of thesis*
L. Andraud	MSc Integrated Electronic Devices, ECL	April - September 2001	CNRS/ECL	100%	Développement en Java d'une plate forme CAO pour systèmes analogiques haute fréquence (*Development of a Java CAD platform for high-frequency analog systems*)
M. Brière	MSc Integrated Electronic Devices, UCB Lyon	January-September 2002	CNRS/ECL	50% with F. Gaffiot	Modélisation comportementale d'un détecteur de fluorescence (*Behavioral modeling of a fluorescence-based biomolecule detector*)
F. Castro Alves Filho	MSc Electronic Engineering, U. Campinas	March-September 2002	CNRS/ECL	100%	Méthodologies de conception de circuits à très haut débit de télécommunications à base de HBT (*Design methodologies for high frequency telecommunication circuits using HBT)*
T. Michalke	MSc Electronic Engineering, TU Darmstadt	March-September 2003	ACI Nanosciences	50% with F. Mieyeville	Modèles comportementaux pour la simulation de réseaux optiques intégrés reconfigurables en longueur d'onde (*Behavioral models for the simulation of on-chip wavelength-reconfigurable networks*)
P. Lisik	MSc Electronic Engineering, TU Lodz	April-September 2003	Polonium	100%	Optimization algorithms for analog EDA
M. Owczarek	MSc Electronic Engineering, TU Lodz	April-September 2003	Polonium	100%	Graphical user interface for analog EDA tool
R. Bonnet	MSc Engineering, ECAM	March-September 2004	Région Rhône-Alpes	50% with F. Mieyeville	Etude, modélisation et conception de la partie RF d'un central d'information automobile embarqué (*Analysis, modeling and design of RF blocks in an automotive information system*)
H. Nguyen Huu	MSc Engineering, ECL	April-September 2004	Région Rhône-Alpes	100%	Méthodes hiérarchiques de conception de SoCs extrêmement hétérogènes (*Hierarchical design methods for extremely heterogeneous SoC)*
E. Mastreani	MSc Integrated Electronic Devices, INSA Lyon	January - September 2005	Région Rhône-Alpes	50% with L. Quiquerez	Dimensionnement automatique de microsystèmes biomédicaux (*Automated sizing of biomedical microsystems*)
R. Du	MSc Integrated Electronic Devices, ECL	April – September 2005	SNECMA	100%	Méthodes de conception de microsystème pour l'aéronautique (*Design methods for aeronautical microsystems*)
G. Revy	MSc Computer Science, UT Belfort-Montbéliard	April – September 2005	Région Rhône-Alpes	100%	Interfaces pour l'optimisation hiérarchique de systèmes hétérogènes (*Interfaces for hierarchical optimization of heterogeneous systems*)
X. Yang	MSc Integrated Electronic Devices, ECL	January - September 2007	ANR^{PNANO}	50% with I. Hassoune	Architectures d'additionneur 16-bit à base de DGMOS à grilles asymétriques (*16-bit asymmetric DGMOS-based adder architectures*)
N. Darbinyan	MSc Business Administration, Université Lyon 3	March - September 2007	Nano2008	100%	Modélisation de méthodes de conception pour systèmes sur puce hétérogènes (*Design process modeling for heterogeneous systems on chip*)
P.E. Gaillardon	MSc Integrated Electronic Devices, INSA Lyon	April - September 2008	CPE	50% with R. Daviot	Architectures logiques à base de portes reconfigurables nanoélectroniques (*Logic architectures using reconfigurable nanoelectronic gates*)
P. Piotrow	MSc Electronic Engineering, TU Lodz	April-September 2009	Polonium	100%	Reconfigurable nanocell matrices and functions

[1] The percentages in the following tables indicate my amount of participation in the role of supervision and training: definition and orientation of topics and objectives, day-to-day supervision and verification of final results, manuscripts and publications.

PhD students

Name	*Nature of degree*	*Period*	*Funding / Scholarship*	*% co-supervision*	*Title of thesis*
F. Mieyeville	PhD Integrated Electronic Devices, ECL. Defended on 30th October 2001.	September 1998 – October 2001	MENRT	30% with F. Gaffiot and G. Jacquemod, principal advisors	Modélisation de liaisons optiques inter- et intra-puces à haut-débit (*Modeling of high data rate inter- and intra-chip links*)
G. Tosik	PhD Integrated Electronic Devices, ECL. Defended on 28th January 2004.	September 2000 – September 2003	MENRT	50% with F. Gaffiot, principal advisor	Conception et modélisation de la répartition de l'horloge des systèmes intégrés par voie optique (*Design and modeling of integrated optical clock distribution systems*)
F. Tissafi-Drissi	PhD Integrated Electronic Devices, ECL. Defended on 13th December 2004.	September 2001 – December 2004	MENRT	75% with F. Gaffiot, principal advisor	Méthodes et outils de synthèse pour systèmes multi-domaine (*Synthesis methods and tools for multi-domain systems*)
M. Brière	PhD Integrated Electronic Devices, ECL. Defended on 29th November 2005.	September 2002 – September 2005	MENRT	50% with F. Gaffiot, principal advisor	Réseaux sur puce reconfigurables en longueur d'onde (*Wavelength-reconfigurable networks on chip*)
S. Dia	PhD Integrated Electronic Devices, ECL. Defended on 19th December 2006.	October 2003 – October 2006	Région Rhône-Alpes	Principal advisor; 45% with F. Gaffiot and F. Mieyeville	Outils de conception de blocs radiofréquences et optiques dans les systèmes sur puce (*Design tools for RF and optical blocks in systems on chip*)
J. Liu	PhD Integrated Electronic Devices, ECL. Defended on 19th November 2008.	October 2005 – September 2008	MENRT	Principal advisor; 90% with F. Gaffiot	Architectures reconfigurables à base de CNTFET double grille (*Double-gate CNTFET-based reconfigurable architectures*)
H. Filiol	PhD Integrated Electronic Devices, ECL. Defense expected in November 2009.	October 2006 - September 2009	BDI CNRS / CEA	Principal advisor; 50% with D. Morche	Architectures analogiques adaptées aux technologies nanométriques et méthodes de conception associées (*Nanometer technology based analog architectures and associated design methods*)
M. Owczarek	PhD Electronic Engineering, TU Lodz. Defense expected in April 2010.	January 2005 – December 2009	TU Lodz scholarship	30% with F. Gaffiot and Z. Lisik, principal advisor	Computer methods for efficient optimization of photonic systems
P.E. Gaillardon	PhD Integrated Electronic Devices, ECL. Defense expected in September 2011.	September 2008 – September 2011	CEA	Principal advisor; 50% with F. Clermidy	Architectures de calcul reconfigurables et à base de composants moléculaires (*Reconfigurable computing architectures based on molecular devices)*
J. Kotb	PhD Integrated Electronic Devices, ECL. Defense expected in September 2012.	September 2009 – September 2012	ANR^{ARPEGE} Nanograin	Principal advisor; 100%	Logique reconfigurable à base de CNTFET double grille (*Double-gate CNTFET based reconfigurable logic)*
F. Frantz	PhD Integrated Electronic Devices, ECL. Defense expected in September 2012.	September 2009 – September 2012	CATRENE 3DIM3	Principal advisor; 100%	Méthodes et outils pour l'exploration des architectures hétérogènes 3D *(3D heterogeneous architectural exploration methods and tools)*
V. Viswanathan	PhD Integrated Electronic Devices, ECL. Defense expected in September 2012.	October 2009 – October 2012	ANR^{PNANO} 3D-IDEAS	Principal advisor; 50% with D. Navarro	Méthodes et outils de conception d'imageurs en technologies d'intégration 3D (*Modeling and design methods for 3D imager ICs*)
M. Galos	PhD Integrated Electronic Devices, ECL. Defense expected in September 2012.	October 2009 – October 2012	MENRT	Principal co-advisor; 10% with C. Gehin	Réseaux de capteurs sans fil pour applications médicales (*Wireless sensor networks for medical applications*)

Postdoctoral research associates

Name	*Period*	*Funding*	*% co-supervision*	*Topic*
E. Drouard	September 2003 – August 2004	CNRS-STIC	50% with X. Letartre	Reconfigurable photonic networks for optical interconnections in microelectronics
F. Tissafi-Drissi	January 2005 – December 2005	FP6-IST-PICMOS	100%	Models and design methods for integrated optical interconnect
I. Hassoune	June 2006 - July 2007	ANR^{PNANO} Multigrilles	50% with D. Navarro	Design of novel logic cells based on double-gate MOSFETs
S. Burignat	September 2006 - August 2007	CNRS-ST2I	100%	Exploration of nanosystem architectures
H. Charlery	March 2007 - January 2008	Nano2008 / STMicroelectronics	100%	Predictive design methods for heterogeneous systems on chip
A. Allam	September 2008-August 2010	FP7-ICT-WADIMOS	50% with F. Mieyeville	Optical interconnect for Multiprocessor SoC
L. Labrak	January 2009-January 2010	Nano2013 / STMicroelectronics	100%	Predictive design for heterogeneous 3D ICs
B. Wang	April 2009-March 2011	FP7-ICT-HELIOS	50% with E. Drouard	Modeling and design methods for Photonics on CMOS
N. Yakymets	June 2009-May 2011	ANR^{ARPEGE} Nanograin	100%	Nanoreconfigurable circuit design technology

Participation in examination boards

PhDs external to ECL

Name	*Date*	*University / Principal advisor*	*Role*	*Title of thesis*
D. Navarro	17th October 2003	Université Montpellier II / Prof. G. Cambon	Invited member	Architecture et conception de rétines silicium CMOS: Application à la mesure du flot optique
S. Riso	28th November 2005	Université de Montpellier II / Prof. M. Robert	Reviewer	Evaluation des paramètres architecturaux des réseaux sur puce
A. Andriahantenaina	16th December 2005	Université de Paris VI / Prof. A. Greiner	Reviewer	Implémentation matérielle d'un micro-réseau SPIN à 32 ports
O. Tintori	15th December 2006	Université de Provence, Aix-Marseille I / Prof. J.L. Autran	Reviewer	Modélisation et simulation des transistors Double-Grille : du dispositif au circuit intégré
N. Lhostis	20th June 2007	Ecole Nationale Supérieure de Télécommunications de Paris / Prof. A. Amara	Reviewer	Techniques et méthodes de conception basse consommation en technologie SOI
M. Oyamada	23rd October 2007	Institut National Polytechnique de Grenoble / A. Jerraya	Reviewer	Estimation de performance du logiciel en systèmes multiprocesseur monopuces
A. Zenati	26th October 2007	Université Joseph Fourier, Grenoble / Prof. S. Basrour	Reviewer	Modélisation et simulation de microsystèmes multi domaines à signaux mixtes : vers le prototypage virtuel d'un microsystème autonome
T. Levi	4th December 2007	Université Bordeaux I / Prof. P. Fouillat	Reviewer	Méthodologie de développement d'une bibliothèque d'IP-AMS en vue de la conception automatisée de systèmes sur puces analogiques et mixtes
A. Tournier	18th December 2007	Université Lyon I / Prof. G.N. Lu	Chairman	Pixel 1-Transistor à modulation de charges pour capteurs d'images CMOS à haute résolution
N. Bruchon	19th December 2007	Université Montpellier II / Prof. L. Torres	Reviewer	Evaluation, validation and design of hybrid CMOS – non-volatile emerging technology cells for dynamically reconfigurable fine grain architecture
Y. Joannon	11th April 2008	Institut Polytechnique de Grenoble / Prof. S. Tedjini	Reviewer	Qualification et génération automatique de stimuli pour le test de systèmes sur puces (SoC) analogiques mixtes et RF
J. Cornet	25th April 2008	Institut Polytechnique de Grenoble / Prof. F. Maraninchi	Member	Separation of Functional and Non-Functional Aspects in Transactional Level Models of Systems-on-Chip
W. Heirman	30th May 2008	Universiteit Gent / Prof. J. Van Campenhout	Reviewer	Reconfigurable optical interconnection networks for shared-memory multiprocessor architectures
Y. Layouni	10th July 2008	INSA Lyon / Prof. N. Abouchi	Chairman	Synthèse architecturale de convertisseurs sigma-delta
B. Zongo	3rd September 2008	Institut Polytechnique de Grenoble / Prof. J.M. Fournier	Reviewer	Méthodologie de conception analogique appliquée à un régulateur de tension à faible chute de tension (LDO)
B. Nicolle	11th September 2008	Université de Nice-Sophia Antipolis / Prof. G. Jacquemod	Member	Optimisation et validation de spécifications pour transmetteurs multi-standards
G. Terrasson	24th November 2008	Université de Bordeaux / Prof. S. Basrour	Member	Contribution a la conception d'un émetteur-récepteur pour microcapteurs autonomes
A. Lewicki	1st December 2008	Université de Nice-Sophia Antipolis / Prof. G. Jacquemod	Reviewer	Conception de modèles haut-niveau pour l'optimisation et la vérification de systèmes Bluetooth
X. Loussier	12th December 2008	Université de Provence (Aix-Marseille I) / Dr. D. Munteanu	Chairman	Modélisation et simulation analytique et numérique des nano-transistors multi-grille : du dispositif au circuit intégré
B. Dubois	3rd July 2009	Université de Strasbourg / Prof. F. Braun	Reviewer	Méthodologie de conception de magnétomètre dans une approche mécatronique
O. Leman	11th September 2009	Université de Montpellier 2 / Prof. P. Nouet	Reviewer	Modélisation et conception d'interfaces faible bruit pour capteurs thermiques micro-usinés : application aux accéléromètres convectifs

J. Goguet	30th September 2009	Université de Bordeaux / Prof. T. Zimmer	Reviewer	Modélisation compacte du transistor à nanotube de carbone à double grille
S. Jovanovic	6th November 2009	Université de Nancy 1 / Prof. S. Weber	Reviewer	Architecture reconfigurable de système embarqué auto-organisé
F. Guigues		Université de Provence Sud Toulon Var / Prof. H. Barthélemy	Reviewer	Conception de structures analogiques 'nanowatt' en technologie CMOS standard

Professoral dissertations

Name	*Date*	*University*	*Role*	*Title of thesis*
C. Seassal	9th March 2007	Ecole Centrale de Lyon	Member	Micro-Nanophotonique active III-V/silicium à base de cristaux photoniques et de microdisques
X. Letartre	3rd June 2008	Ecole Centrale de Lyon	Member	Micro et nano structures de semiconducteurs pour la micro-opto-électronique
J.O. Klein	30th April 2009	Université Paris Sud 11	Reviewer	Impact des technologies sur les architectures de calcul
P. Maurine	10th December 2009	Université Montpellier 2	Reviewer	Contribution à la modélisation et à la robustesse des circuits intégrés CMOS en technologie nanométrique

Principal responsibilities in scientific programs

Regional projects (Rhône-Alpes)

Project acronym / Program	*Period*	*Coordination*	*Role*	*Total funding / partner funding*	*Full title of project*
Osmose	2003-2006	ECL	Coordinator Leader for WP4 (Synthesis and design methods)	210K€ / 133K€	Outils pour la co-simulation, synthèse et modélisation de systèmes sur puce (*Tools for co-simulation, synthesis and modeling of systems on chip*)
EmSoC-Recherche	2004-2007	INP Grenoble	Leader for WP6 (Hardware architectures and heterogeneous design)	200K€ / 15K€	Systèmes embarqués (*Embedded systems*)
SEMBA	2008-2011	INP Grenoble	Leader for WP3 (Communication infrastructures for smart objects)	200K€ / 15K€	Systèmes embarqués (*Embedded systems*)

National projects (France)

Project acronym / Program	*Period*	*Coordination*	*Role*	*Total funding / partner funding*	*Full title of project*
Heteropt / RMNT	2001-2004	ECL	Leader for WP5 (Circuit design)	450K€ / 50K€	New technologies for heterogeneous integration of high-density optical links on silicon integrate circuits
Nanosys / ACI Nanosciences	2004-2006	IEF	Leader for WP2 (Elementary nanodevice-based functions)	300K€ / 25K€	Architectures for the integration of molecular nanodevices
Multigrilles / ANR^{PNANO}	2005-2007	CEA-LETI	Leader for WP3 (Design of novel digital and analog cells)	800K€ / 100K€	Disruptive design of elementary cells for multiple gate sub 32nm CMOS circuits
3D-IDEAS / ANR^{PNANO}	2008-2011	ECL	Coordination Leader for WP2 (Design flow)	1.5M€ / 300K€	3D integration and design technology for imager applications and systems
Nanograin / ANR^{ARPEGE}	2008-2011	CEA-LETI	Leader for WP2 (Nanograin cells and associated functions)	500K€ / 200K€	Ultra-fine grain reconfigurable architectures based on nanodevices

European projects

Project acronym / Program	*Period*	*Coordination*	*Role*	*Total funding / partner funding*	*Full title of project*
PICMOS / FP6-IST-STReP	2004-2007	IMEC (BE)	Leader for WP1 (System studies, Definition of applications)	2M€ / 100K€	Photonic Integration on CMOS
WADIMOS / FP7-ICT-STReP	2007-2010	IMEC (BE)	Joint leader for WP1	2.2M€ / 240K€	Wavelength Division Multiplexed Photonic Layer on CMOS
HELIOS / FP7-ICT-IP	2008-2012	CEA-LETI (FR)	Leader for WP7.1	5M€ / 200K€	Photonics Electronics functional integration on CMOS
3DIM3 / Eureka-CATRENE	2008-2012	STMicroelectronics (FR)	INL coordinator	15M€ / 350K€	3D-TSV Integration for Multimedia and Mobile Applications

International projects

Project acronym / Program	*Period*	*Coordination*	*Role*	*Total funding / partner funding*	*Full title of project*
DMT / PICS CNRS	2008-2010	ECL / EPM	French partner coordination	45K€ / 22K€	Design methods and tools for future heterogeneous system on chip architectures